

CP-642B MEMORY ADDRESS ASSIGNMENT

OCTAL ADDRESS RANGE		USE
00000 - 00000		Fault Entrance Address (With AUTOMATIC RECOVERY switch in center position) — illegal instruction code or illegal use of control memory
Core Memory	00001 - 00017 00020 - 00037 00040 - 00057 00060 - 00077	Unassigned External Interrupt Entrance Addresses Input Monitor Interrupt Entrance Addresses Output Monitor Interrupt Entrance Addresses
Control Memory	00100 - 00117 00120 - 00137 00140 - 00157 00160 - 00180 00161 - 00167 00170 - 00177	Input Buffer Control Words Output Buffer Control Words External Function Buffer Control Words Real-Time Clock B-Registers Unassigned
Core Memory	00200 - 00477 00500 - 00517 00520 - 00537	Unassigned External Function Buffer Monitor Interrupt Entrance Addresses Interrupt Word Storage Address
	00540 - 00577	Bootstrap - Wired Memory
Core Memory	00600 - 00617 00620 - 77777	Intercomputer Time Out Interrupt Entrance Address Unassigned

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UNIVAC CP-642B COMPUTER REPERTOIRE OF INSTRUCTIONS

SPERRY RAND CORPORATION
UNIVAC
Defense Systems Division

i01	Right SHIFT ^Q	Shift (Q) Right by Y
f02	Right SHIFT ^A	Shift (A) Right by Y
f03	Right SHIFT ^{AQ}	Shift (AQ) Right by Y
*f04	COMpare ^{A,*Q,*AQ}	Sense (j); $A_1 = A_2$
i05	Left SHIFT ^Q	Shift (Q) Left by Y
i06	Left SHIFT ^A	Shift (A) Left by Y
i07	Left SHIFT ^{AQ}	Shift (AQ) Left by Y
f10	ENTER ^Q	$Y \rightarrow Q$
f10	CLEAR ^A	$\bar{Y} \rightarrow A$
f11	ENTER ^{BP}	$\bar{Y}=0, Y \rightarrow A$
f12	CLEAR ^{BN}	$\bar{Y}=0, Y \rightarrow B$
f12	NO-OPeration	$\bar{Y}=0, Y \rightarrow B$
$\wedge f13k0$	EXternal-COMmand ^{(C^n*W(Y))*MONITOR}	Enter B^0 with 0 (do nothing operation)
$\wedge f13k1$	EXCom-COMmand ^{(C^n*W(Y))*MONFORCE}	$(Y) \rightarrow C^1$; (to be used on all CP-642A/USQ-20 peripheral equipment), (Interrupt at 00500+)
$\wedge f13k2$	EXternal-COMmand ^{(C^n*W(Y))}	$(Y) \rightarrow C^1$; (to be used on all CP-642A/USQ-20 peripheral equipment)
$\wedge f13k3$	EXternal-COMmand ^{(C^n*W(Y))*FORCE}	$(Q) \rightarrow C^1$
i14	SToRe ^Q	When $Y = Q$; then $Q' \rightarrow Q$
i14k0	ComPlement ^{•Q}	$(A) \rightarrow Y$
i15	SToRe ^A	$(B) \rightarrow Y$
i16	SToRe ^{BN}	Jump to \bar{Y} if external function buffer active
$\wedge f17k0$	Jump ^{P*Y*C^n*COMACTIVE}	Jump to $L(Y)*C^n*COMACTIVE$
$\wedge f17k1$	Jump ^{L(Y)*C^n*COMACTIVE}	Jump to $L(Y)$ if external function buffer active
$\wedge f17k2$	SToRe ^{C^n*W(Y)}	00520- $\bar{Y} \rightarrow (Y)$
$\wedge f17k2$	SToRe ^{C^n*W(Y)*FORCE}	Force $C^1 \rightarrow (Y)$ - (abnormal test mode)
i20	ADD ^A	$(A) \rightarrow Y$
i21	SUBtract ^A	$(A) \rightarrow Y$
i22	MULtiply	$(Q) \rightarrow AQ$
*i23	DIVide	$(AQ) \rightarrow Y; R \rightarrow Ar$
*i23k7	SSquare Root ^T	$\sqrt{Q} \rightarrow Q;$ remainder $\rightarrow A$
i24	RePlace ^{A-Y}	$(A)-Y \rightarrow Y\&A$
i25	RePlace ^{A+Y}	$(A)+Y \rightarrow Y\&A$
*i26	ADD ^Q	$(Q)-Y \rightarrow Q$
*i27	SUBtract ^Q	$(Q)+Y \rightarrow Q$
i30	ENTER ^{X-Q}	$\bar{Y}-Q \rightarrow A$
i31	ENTER ^{X-Q}	$\bar{Y}-Q \rightarrow A$
i32	SToRe ^{A-Q}	$(A)-Q \rightarrow Y\&A$
i33	SToRe ^{A-Q}	$(Y)+Q \rightarrow Y\&A$
i34	RePlace ^{A-Q}	$(Y)-Q \rightarrow Y\&A$
i35	RePlace ^{X-Q}	$(Y)-Q \rightarrow Y\&A$
i36	RePlace ^{X-Y}	$(Y)-I \rightarrow Y\&A$
i37	RePlace ^{X-Y}	$(Y)-I \rightarrow Y\&A$
*i40	ENTER ^{LP}	$L(\bar{Y}(Q)) \rightarrow A$
i41	ADD ^{LP}	$(A)-L(\bar{Y}(Q)) \rightarrow A$
i42	SUBtract ^{LP}	$(A)-L(\bar{Y}(Q)) \rightarrow A$
i43	COMpare ^{=MASK}	$(A)-L(\bar{Y}(Q)) \rightarrow A$
*i44	RePlace ^{LP}	$L(\bar{Y}(Q)) \rightarrow Y\&A$
i45	RePlace ^{A-LP}	$L(\bar{Y}(Q)-A) \rightarrow Y\&A$
i46	RePlace ^{A-LP}	$(A)-L(\bar{Y}(Q)) \rightarrow Y\&A$

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147	SToRe*LP	L(A)(Q) → Y; (A) ₁ = (A) _f
150	SELective*SET	Set (A) _n for Y _n = 1
151	SElectiveComPlement	COMPLEMENT (A) _n for Y _n = 1
151k4	Complement*A	When Y is 77777, then A' → A
152	SELective*Clear	Clear (A) _n for Y _n = 1
153	SELective*Subtract	A _n → A _n - (Q) _n = 1
154	Replace SELective*SET	Set (A) _n for (Y) _n = 1
155	Replace SELective*SET	COMPLEMENT (A) _n for (Y) _n = 1 → Y&A
156	Replace SELective*CL	Clear (A) _n for (Y) _n = 1 → Y&A
157	Replace SELective*SU	(Y) _n → (A) _n for (Q) _n = 1, → Y
160	Jump (arithmetic)	Jump to Y if jump j-condition is satisfied
160j0	Remove Interrupt Lockout	RIL on all internal channels and all external channels not locked out by SEL-EX
160j1	Remove Interrupt Lockout Jump*W	RIL; jump to Y
161	Jump (manual)	Jump to Y if jump j-condition is satisfied
162	Jump* [(if C ⁿ has ACTIVE INput buffer)	Jump to Y if C ⁿ input buffer active
163	Jump* [(if C ⁿ has ACTIVE OUTput buffer)	Jump to Y if C ⁿ output buffer active
164	Return Jump (arithmetic)	Jump to Y+1 and P+1 → Y ₁ if j-condition is satisfied (see JP & RJP j-designators)
165	Return Jump (manual)	Terminates input buffer on C ^j
*166	TERMinate*Cn*INPUT	RIL on all internal channels and all external channels not locked out by SEL-EX
*166k1	Remove Interrupt Lockout*ALL	Remove interrupt on all channels
*166k2	Remove Interrupt Lockout*External*ALL	RIL for external interrupts on all channels
*166k3	Remove Interrupt Lockout*External*C ^j	RIL for external interrupts on C ^j
*166k1b1	Set Interrupt Lockout*ALL	Sets external and internal lockout on all channels
*166k2b1	Set Interrupt Lockout*External*ALL	Sets external interrupt lockout on all channels
*166k3b1	Set Interrupt Lockout*External*C ^j	Sets external interrupt lockout on C ^j
*167	TERMinate*Cn*OUTPUT	Terminates output buffer on C ^j
*167k1	TERMinate*Cn*COMMAND	Terminates external function buffer on C ^j
*167k2	TERMinate*ALL buffers	Terminates all buffers
*170	RePeat	Executes NI Y times
171	BSKip*BP	(B) _j =Y, skip NI and clear (B) _j , (B) _j ≠Y, advance B _j and read NI
172	BJump*BP ⁿ	(B) _j =0, read NI; (B) _j ≠0, (B) _j -1 and jump to address Y
*173	INput*C ⁿ (without monitor mode)	Buffer IN on C ^j ; buffer control word → 00100- ^j
*174	OUTput*C ⁿ (without monitor mode)	Buffer OUT on C ^j ; buffer control address → 00120- ^j
*174k2	EXternal-COMmand-MultiWord*C ⁿ *W(Y)	Buffer out on C ^j ; (Y) → (00140- ^j)
*175	INput*C ⁿ (with*MONITOR mode)	Buffer IN on C ^j with monitor; buffer control word → 00100- ^j ; monitor interrupt address → (00040- ^j)
*176	OUTput*C ⁿ (with MONITOR mode)	Buffer OUT on C ^j with monitor; buffer control address → 00120- ^j ; monitor interrupt address → (00060- ^j)
*176k2	EXternal-COMmand-MultiWord*C ⁿ *W(Y)*MONITOR	Buffer OUT on C ^j ; interrupt at → (00500- ^j)

* } Special j and k designators

Y - The operand; Y or Y₁

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JP & RJP j-DESIGNATORS

j	JP 160	RJP 164	JP 161	RJP 165
0	(No Jump)	(Uncond. Jump)*	(Uncond. Jump)	
1		(Uncond. Jump)*	KEY 1	
2	Q POS		KEY 2	
3	Q NEG		KEY 3	
4	A ZERO		STOP	
5	A NOT zero		STOP 5	
6	A POS		STOP 6	
7	A NEG		STOP 7	
8	62	63		
9-17	C ⁿ ACTIVE IN	C ⁿ ACTIVE OUT		

*0 Clears interrupt & bootstrap modes.

^ J-DESIGNATORS & K-DESIGNATORS

^ Occupies 4 bit positions and represents Cⁿ where n may be 0-17₈.

^ Controls operand interpretation, it is limited to 2 bit positions since the j-designator requires 4 bits.

The instruction word assumes the format:

t	^	^	k	b	y
29-	-24	-23	-20	19	18 17 - 15 14- -0

^ J-DESIGNATORS

j	COM*A . *Q . *AQ	DEV 104	DEV f23	ADD Q, SUB Q	ENT*LP, RPL*LP	RPT 170	SQRT f23 k7
0	(no skip)	(no skip)	(no skip)	(no skip)	(no mod.); Y of NE = Y	(no skip)	
1	(unconditional skip)	SKIP	SKIP	SKIP	ADV : Y of NE = Y+1	SKIP	
2	Y LESS : Y ≤ (Q)	NO OverFlow	A POS	EVEN parity	BACK : Y of NE = Y-1	REM	
3	Y MORE : Y ≥ (Q)	OverFlow	A NEG	ODD parity	ADD B : Y of NE = Y+B ⁸	NO REM	
4	Y IN : (Q) ≤ Y and Y ≥ (A)	A ZERO	Q ZERO	A ZERO	Rpl. Inc.: Y of NE = Y+B ⁸	✓ not used	
5	Y OUT : (Q) ≤ Y or Y ≤ (A)	A NOT zero	Q NOT zero	A NOT zero	ADV R : Y of NE = Y+1.B ⁸	✓ not used	
6	Y LESS : Y ≤ (A)	A POS	Q POS	A POS	BACK R : Y of NE = Y-1.B ⁸	✓ not used	
7	Y MORE : Y > (A)	A NEG	Q NEG	A NEG	ADD B R : Y of NE = Y+B ⁸	✓ not used	

✓⁸ Increment if NI is RPL class; increments Y address for the store portion of the replace.

NE - Next execution

NORMAL j-DESIGNATORS

j	READ		STORE		REPLACE
k	Code	Origin	Code	Origin	Dest.
0	"blank"	U _L	Q	Q	'not used'
1	SKIP				
2	Q POS	U	M _L	L	M _L
3	Q NEG	U	M _L	U	M _U
4	A ZERO	W	W	W	M
5	A NOT zero	X _{UL}	A	'not used'	-
6	A POS	LX _{ML}	CPL	CPL M _L	LX _{ML}
7	A NEG	UX _{ML}	CPL	CPL M _U	UX _{ML}

NORMAL k-DESIGNATORS

k	READ		STORE		REPLACE
j	Code	Origin	Code	Origin	Dest.
0	"blank"	U _L	Q	Q	'not used'
1	SKIP				
2	Q POS	U	M _L	L	M _L
3	Q NEG	U	M _L	U	M _U
4	A ZERO	W	W	W	M
5	A NOT zero	X _{UL}	A	'not used'	-
6	A POS	LX _{ML}	CPL	CPL M _L	LX _{ML}
7	A NEG	UX _{ML}	CPL	CPL M _U	UX _{ML}

LEGEND

- M - Memory word (30 bits)
- M₁ - Lower half memory word
- M_U - Upper half memory word
- X - Sign bit extended
- CPL - Complement
- A - A-register
- Q - Q-register