UNIVAC to UNISYS TECHNOLOGIES

Compiled and Transcribed by B. N. 'Mike' Svendsen

Engineering Highlights of the 80s
Are Exhibited on the History Wall.

2470 Highcrest Road - Roseville, MN 55113

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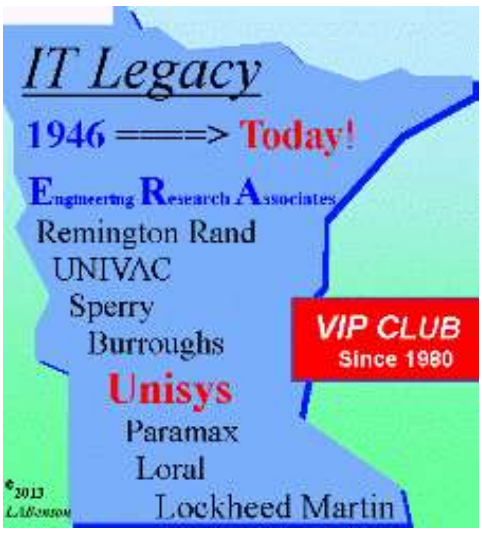
The file name of this paper is univac2unisys; we documented the processor lineage parts of the history wall in file ERA2unisys.

UNIVAC to UNISYS TECHNOLOGIES

INTRODUCTION

Sperry-UNIVAC management in Roseville had a sense of history thus began to illustrate their computer technologies with a series of wall mounted shadow box displays. Harry Smuda (management) and Dick Petschauer (engineering) created the original shadow boxes. After the Burroughs buyout of Sperry in 1986; the resulting UNISYS Company kept the displays.

In 1946; Engineering Research Associates started an amazing legacy of Information Technology (IT) in Minnesota. In 2005, the UNISYS and Lockheed Martin retirees club started a Legacy Committee with the expressed purpose of preserving this fascinating history.



This paper illustrates and documents the contents of Fiscal Year (FY) 'history' shadow boxes for research by computer technology historians. The plaque text within each shadow box as transcribed by Mike Svendsen is in the various sections hereunder.

COMPUTER TECHNOLOGY EVOLUTION

The Legacy Committee is passionate about preserving these technologies of the 80s as parts of our Information Technology Legacy. Portions of this paper's sections were associated with developments at the Sperry Univac semi-conductor facility in Eagan which was closed two years after Burroughs bought Sperry to form UNISYS.

FY ’79 Engineering Highlights:

FIRST STORAGE PC BOARD LAYOUTS - The first application of the storage PC board layout (automated placement and routing) capabilities of UCADS (Univac Computer Aided Design System) occurred during FY’79. A multilayer board (4-signal, 2-pad, voltage and ground layers), utilizing TTL technology, was designed for the Type 7050 Storage system. Previous CAD systems did not satisfy the unique physical requirements of double sided Storage board design and manual layout has historically been used for these applications. Using UCADS, a cost effective multilayer design was produced, with better documentation, and with faster turn-around time on revisions, than could be done using manual methods.

1100/60 SYSTEM - This newest member of the 1100 series, three years in development, is scheduled for public announcement in early FY ’80. The 1100/60 processor uses LSI microprocessor chips to implement a unique multiprocessor design to achieve outstanding performance and reliability at the lower cost end of the 1100 line. Major milestones during FY’79 included the Development Release of product documentation, demonstrations of 1x1

system operation with DVR and MATE (test software), the 2x2 system with DVR software, and attainment of hardware stability in support of System Software Development.

FIRST SPERRY UNIVAC BIPOLAR IC- The total capability of producing sample quantities of Bi-Polar Integrated Circuit (IC) logic devices within Sperry Univac St. Paul Operations (Roseville and Eagan) was successfully demonstrated. The Bi-Polar device, designated BT106 uses SNECL (Sub-Nanosecond Emitter Coupled Logic) technology, and provides five two-input OR/NOR gates with common enable in a 24-pin leadless package. (*24-pin leadless flat package with BT-106 die mounted and lid not applied- IC silicon wafer containing 2480 chips).*

SAM GATE ARRAYS - First use of the Gate Array (a versatile, high density, low cost, logic circuit configuration) in a Sperry Univac product design was in the SAM (Scientific Accelerator Module) Unit. SAM, a high speed, scientific-oriented processor for the 1100 Series systems, uses 126 Gate Array chips of10 different types, on 22 pc-boards.

SPERRY UNIVAC SCIENTIFIC PROCESSOR - The Univac Scientific Processor (USP) is a special purpose processor with arithmetic capabilities oriented toward scientific computation. It is intended to operate in a multiprocessor environment, with at least one standard CPU, in the next generation 1100 series system. The USP architectural design, defining primarily its functional and programming characteristics, was completed during this fiscal year.

LSI ANALYSIS LABORATORY - An LSI (Large Scale Integration) analysis laboratory was established in FY'79. The laboratory is equipped with a variety of instruments, optical devices, and a photographic laboratory, for dissection and analysis of LSI semi-conductor devices. A Scanning Electron Microscope (SEM) will be added in the coming year.

HIGH PERFORMANCE PACKAGING - A High Performance Packaging System (HPP) is being developed for use with next generation Sperry Univac computer system in the 1980's. This high speed and high density electronic hardware uses Gate Arrays, 100K ECL circuits, custom IC (Integrated Circuit) packages, dense multilayer logic boards with connections on three sides, and liquid cooling. During FY'79 the definition, feasibility studies, and first prototypes of HPP hardware components were completed.

SUL 2 STORAGE - The prototype of the storage module for SUL-2 system was delivered to General Systems Division, Blue Bell. The storage module uses a "mother/baby" board configuration with 16K chips on the "baby" board. Minimum capacity of the single 18 in. by 20in. "mother" board is 256K bytes, and capacity is expandable to a maximum of 1 million bytes.

SATELLITE LINK ESTABLISHED - A satellite communication link with Blue Bell (later to include Salt Lake City) was established. Ground stations at the two locations communicate via "Westar" stationary satellites located 22,300 miles above the equator. Applications for the link will include digital data for inter-computer communications, freeze-frame high resolution TV,

Telefax, and inter-location conferences. The planned multi-site network will permit evaluation of system communications capability at much higher traffic volumes than are possible with land lines.

FIRST PRODUCTION USE OF UCADS - The first development project use of the total capabilities of UCADS (Univac Computer Aided Design System) was for the Scientific Accelerator Module (SAM). UCADS provided the SAM project with logic representation language, simulation capability, automated logic drawings, pc board layout, pc board and back panel interconnection, artwork, design documentation and test generation. *[Calma designer console-Checking of PC Artwork generated by UCADS-Gerber Plotter uses control tape produced by UCADS-Logic diagram produced by UCADS via COM unit.]*

CACHE-DISK - Roseville Engineering Center and the ISS division of Sperry Univac are jointly developing a disk subsystem utilizing cache [high-speed buffer] storage. The system design and the cache storage unit development were performed at Roseville. The prototype storage system for the cache using 16k RAM chips was shipped to ISS for development work on the subsystem. The T7047 will be superseded by the T7053 storage with capability of using 64K RAM chips.

NUK 1100/80 ARM - ARM (Availability, Reliability, Maintainability) enhancements for the 1100/80 systems in Japan were developed in cooperation with NUK personnel. Development was completed and fifteen modifications kits were shipped to NUK.

FASTRAND COMPATIBLE DISK SUBSYSTEM - The Fastrand-Compatible 5046 Disk Subsystem enables Univac 400 and 1100 series customers to upgrade their mass storage subsystems from present Fastrand drums to Disks with no mandatory change in software. Roseville Custom Engineering developed Fastrand compatibility features for Disk Subsystems, and the 30th unit was delivered in FY'79.

1100/84 4X4 DELIVERY - Delivery of the first 4x4 1100/84 System (maximum 1100/80 configuration) was made to Lufthansa Airways, West Germany's largest airline, where it will be used in all phases of the airline's operation. Installation of the system, and turn over to the customer was accomplished in ten days.

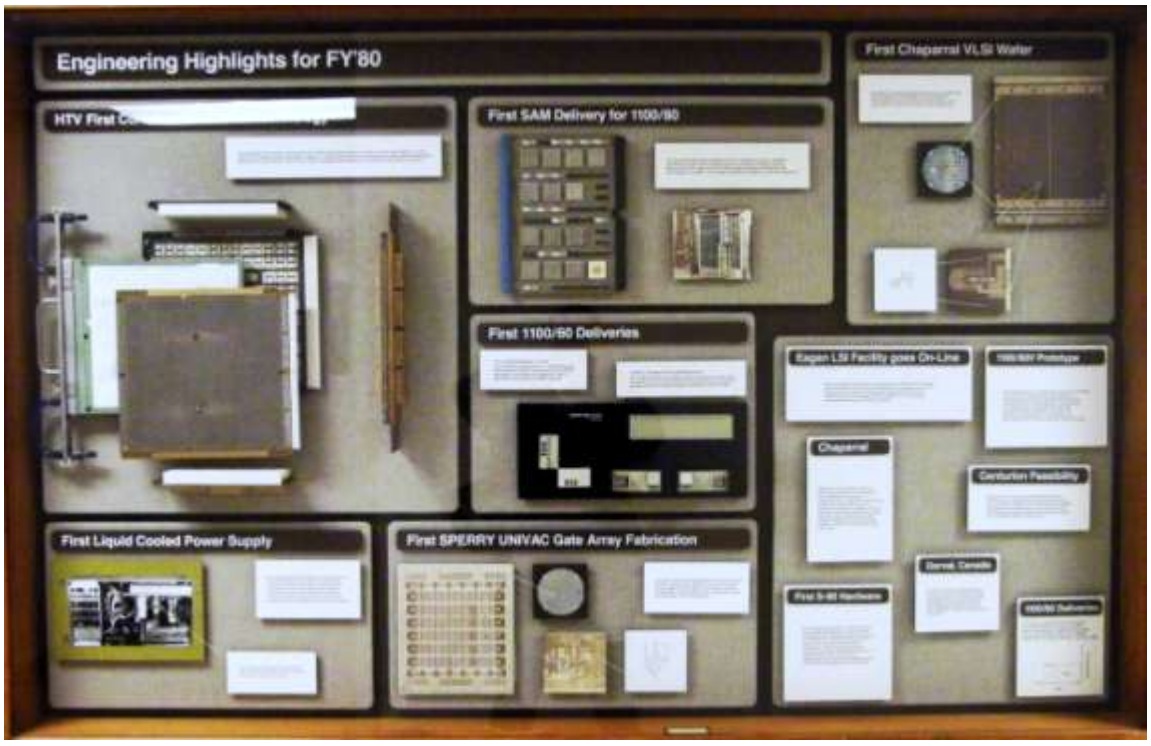
FIRST 64K RAM-1100/64 - Design of the type 7049 Main Storage Unit for the 4x4 1100/64 was initiated during FY'79. This is the first Sperry Univac product to use 65,536- bit [commonly referred to as "64K-bit"] LSI semiconductor devices. One PC card, 9 in. x 10 in., provides 131,072 43- bit (36 data plus 7 ECC) words of storage. Changes to the other 1100/60 central complex units to provide 4x4 capability were also designed and tested this year.

1100/80A - Elements of the 1100/80 system, modified to accommodate the 4x4 configuration, entered the Continuation Engineering Phase. Fully tested designs for the Storage Interface Unit, and System Availability Unit were transferred to Roseville Support Engineering.

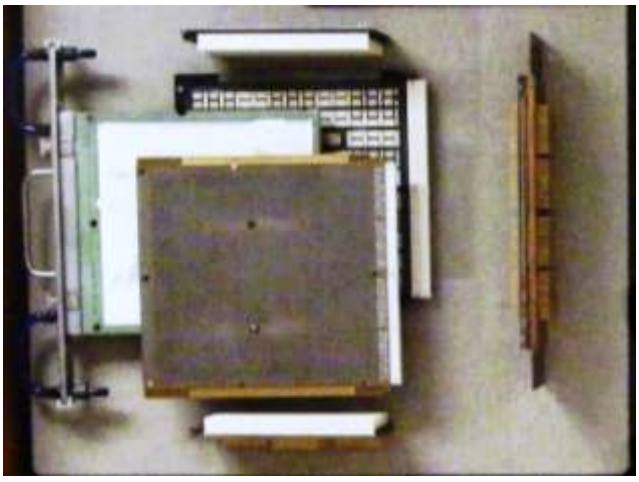
VLSI GATE ARRAY - Design of a VLSI (Very Large Scale Integration) Gate Array circuit for applications requiring moderate performance and low cost (such as entry-level 1100 series) was initiated. Devices being developed will provide up to 1200 gates in a 124-pin package.

INVENTIONS - 47 Invention Disclosures; 58 Inventors- 12 Patent Applications Filed; $3,000 in Awards to 15 Inventors- 4 Patents Issued- First Inventor Recognition Luncheon.

FY ’80 Engineering Highlights:

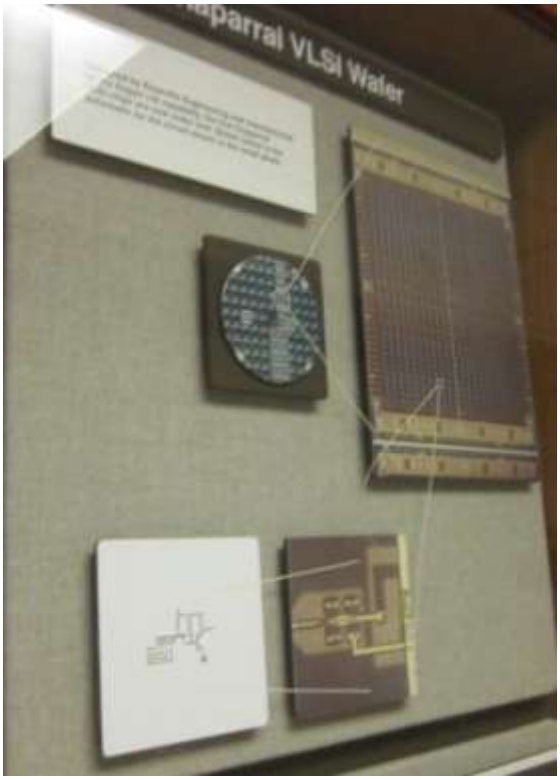


HTV FIRST CONSTRUCTION OF S-80 TECHNOLOGY - The Hardware Test Vehicle (HTV)constructed from S-80’s new sub nanosecond emitter coupled logic (SNECL) is now under test, cooled by water and highly compact in construction. *The basic assembly is a cooling plate sandwiched between two circuit boards with wire-wrap connector*. Twenty-six of these assemblies will comprise the total S-80 instruction processor.



FIRST SAM DELIVERY FOR 1100/80 - The Scientific Accelerator Module for the 1100/80 is a special capability for scientific users and a market expansion product for Sperry Univac. Built from the first gate array LSI logic chips designed in Roseville. The technology is a leader in the design capability needed for the S-80 and Chaparral. *Card assembly with 14 LSI chips.*

FIRST CHAPARRAL VLSI WAFER - Designed by Roseville Engineers and manufactured by the Eagan LSI capability, the first Chaparral VLSI chips are now under test.



FIRST 1100/60 DELIVERIES - The first 46 deliveries of 1100/60 Systems were made in FY80. Current orders for the 1100/60 are equal to 5 years of orders for 1100/11 and that is the product 1100/60 replaces.

1100/62-THE MOST EFFICIENT MULTIPROCESSOR - The 1100/62 is the first multiprocessor to achieve nearly 200% throughput over its unit processor. The previous best and still a close second in multiprocessor efficiency is the 1100/82.

EAGAN LSI FACILITY GOES ON LINE - Now receiving chip designs and layouts from Roseville, the Eagan Semiconductor Facility is manufacturing the prototype parts for Chaparral and Super-80. The Parallel development of future 1100 Systems and the Eagan VLSI capability is an enhancing two-way development for Sperry Univac.

1100/80V PROTOTYPE - The 1100/80 Vectorizer Prototype System is complete. The first stand-alone attached processor for 1100 Systems- since the 1108 attached processor- is developed for 1100/80 Systems. Attachable to all configurations of 1100/80, the resulting product is called 1100/80V. It expands our application capability for the scientific user and expands our customer base for Sperry Univac.

CHAPARRAL - Chaparral is the project with the most new firsts and to accomplish that challenge, the project is organized into a dedicated engineering group. The first product to use production chips from Eagan, the first office environment, and the first large quantity of small peripherals causes Chaparral to be an exciting product aimed at the new entry-level 1100 user.

CENTURION FEASIBILITY - Centurion is a basic new mainframe structure built around an advanced high performance bus and promises a middle range 1100 System at greatly improved cost performance. Under control of the 1100 Operating System Software, the Centurion should be a uniquely capable 1100 product.

FIRST S-80 HARDWARE - An adequate capability for System testing and System maintenance is key to S-80 development in Roseville and S-800 support in the field. The mainframe test network called Scan-set and its associated controllers are developed and in test. Diagnostic software will be added to find failures down to the level of replaceable part, thereby eliminating most of the need to trouble shoot in the field.

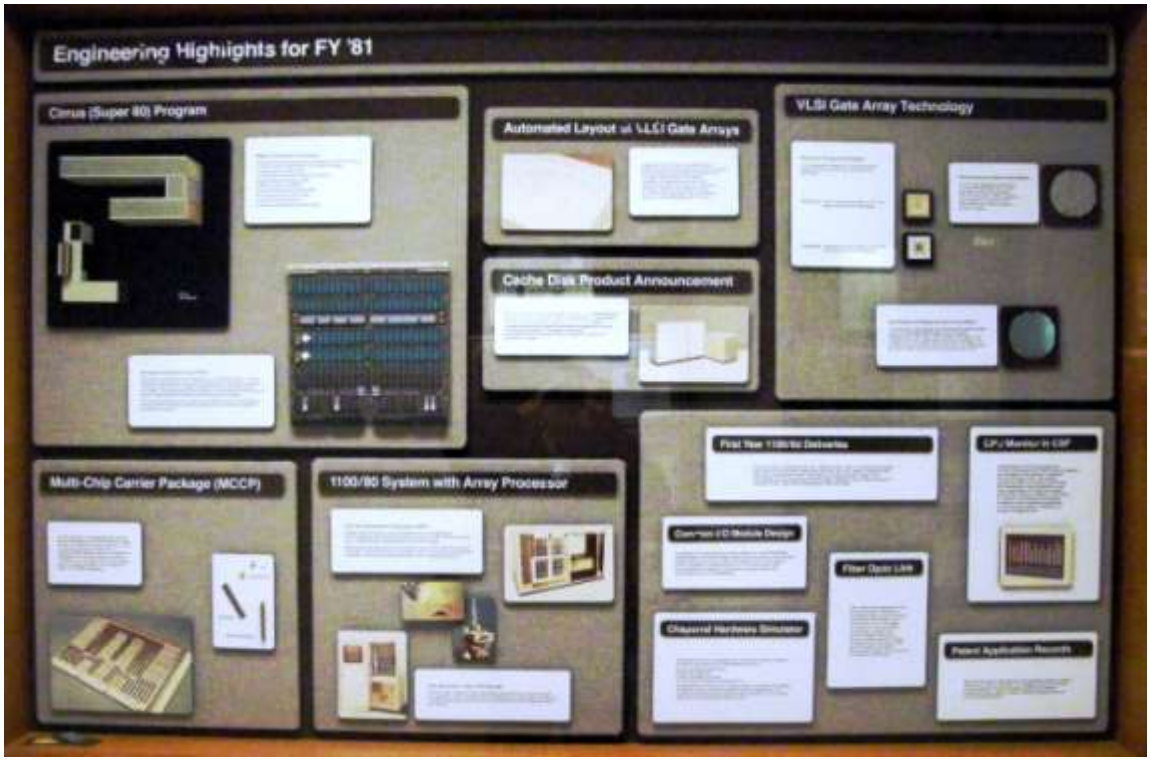
DORVAL, CANADA - For the first time, all of management at Sperry Univac in Dorval, Canada is Canadian. The experience and capability in Dorval that achieved that significant milestone shows the credibility of Sperry's commitment to Dorval.

1100/80 DELIVERIES - At an age younger than half its lifetime, the 1100/80 deliveries have exceeded their business plan. Originally forecasted to sell only 453 processors; the 1100/80 sailed past the magic number in January 1980.

FIRST LIQUID COOLED POWER SUPPLY - The largest S-80 power supply is now under test- an achievement of Sperry Univac facility in Dorval, Canada. The power supply delivers 750 amps for the S-80 instruction processor. Compact in design and efficiently cooled by water, the power supply is the necessary first assembly for the prototype instruction processor.

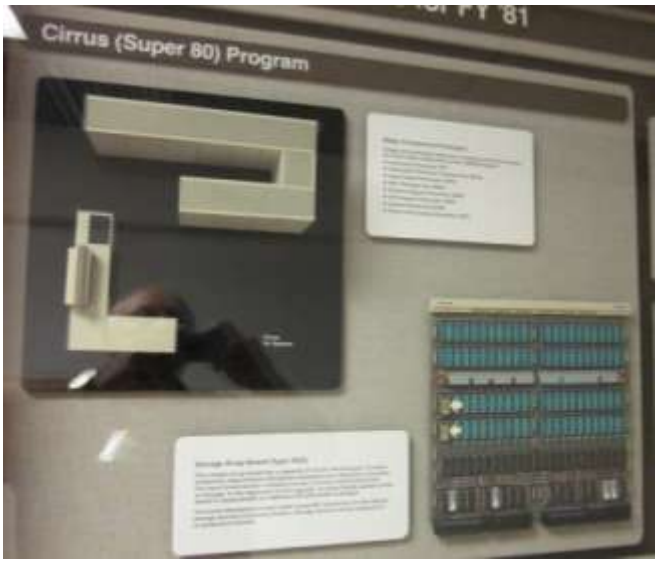
FIRST SPERRY UNIVAC GATE ARRAY FABRICATION - The high speed S-80 chips called sub nanosecond emitter coupled logic (SNECL) are now produced by the Eagan Semiconductor Facility for testing in Roseville.

FY ’81 Engineering Highlights:



Cirrus (Super 80) Program

MAJOR COMPONENT PROTYPES - Design and prototype build was completed and test initiated on these major components of the CIRRUS System. Instruction Processor (IP), Instruction Processor Cooling Unit (IPCU), Input Output Processor (IOP), Main Storage Unit (MSU), System Support Processor (SSP), Unit Support Controller (USC), System Clock Unit (SCU), and Power and Cooling Controller (PCC).



STORAGE ARRAY BOARD (Type 7052) - This unique array board has a capacity of 131,072 44 bit words. To meet modularity requirements the board is designed as a two piece assembly. The basic board section contains common circuitry and 65,536 words of storage. In the expansion to full capacity an outer (blank) portion of the board is replaced with additional 65,536 words of storage. *The board displayed is a test model using DIP connectors*

for the 65K bit storage device (2 devices plugged in). Storage devices will be soldered in on production boards.

AUTOMATED LAYOUT OF VLSI GATE ARRAYS - Capability of the Univac Computer Aided Design System (UCADS) was expanded to include the automated layout (circuit placement and routing) of gate arrays. This added capability will greatly reduce the time required to obtain VLSI parts for computer products. Shown in the adjacent photo is an 80X scale test plot of the metallization layer of the CHAPARRAL ST-101 chip.

VLSI Gate Array Technology

ROSEVILLE DESIGNED PACKAGE - VLSI package designed for specific product applications were built. Two examples are illustrated. CENTURION-132 pin package contains CT-132 gate array die with 1260 gates. CHAPARRAL-138 pin package contains ST-101 gate array die with 1830 gates.

FIRST CENTURION GATE ARRAY WAFERS - The first CT_122 gate array wafers for the CENTURIAN Product were fabricated and testing initiated. The CT-122 is ECL-10K compatible, was designed in Roseville and fabricated at Semiconductor Division in Eagan.

SIZE REDUCED CHAPARRAL GATE ARRAY WAFER - Utilizing new circuit design techniques with tighter design rules, a new CHAPARRAL gate array chip was designed. The new chip is 28% smaller, 30% faster and contains 10% more gates than the previous design. The smaller dimensions also permit more die to be fabricated per wafer, thus improving the overall process yield.

CACHE DISK PRODUCT ANNOUNCEMENT - The Cache Disk Subsystem for 1100/80 and 1100/60 was announced on March 4, 1981. This product was designed jointly by Roseville Major Systems and the ISS. It uses 4 to 64 million bytes of solid state storage in conjunction with an "intelligent" controller to greatly reduce the access time to frequently sought data held on disk.

MULTI-CHIP CARRIER PACKAGE (MCCP) - A new concept in daughter board designs was established for the CENTURION storage module. The MCCP substrate has seven layers of circuitry and mounts eight 65KX1 dynamic ram leadless devices. The MCCP is organized 131KX4 and contains a total of ½ million bits of storage. Use of this concept gives a packing density four times that of dual-in -line (DIP) packaging.

1100/80 System With Array Processor

FIRST ARRAY PROCESSOR SUBSYSTEM (APS) - Design and construction of the first APS for the 1100/80 System were completed and test initiated. Either one or two APS can be attached to an 1100/80 System equipped with Type 7050 storage. Benchmark runs have demonstrated performance 50 to 200 times that of the basic 1100/80 Processor for complete vector calculations such as those required in computation associated with seismic exploration for oil.

FIRST DELIVERY- TYPE 7050 STORAGE - The first eight units of T7050- 1 million words per unit were delivered to a customer. The T7050 Storage is designed to function with the APS in an 1100/80 System and access ports are provided to accommodate two APS per system.

FIRST YEAR 1100/60 DELIVERIES - In the first year of deliveries for the 1100/60 product, 528 1X1 units were shipped, more than 100 above the original business plan. An even higher production rate has been scheduled for FY82. This highly successful product, latest in the

1100 Series, was developed by Roseville Major Systems and is manufactured at Roseville/Clear Lake and Roedelheim, West Germany.

COMMON I/O MODULE DESIGN - A common I/O (Input/Output) module design for the CHAPARRAL, CENTURION and CAPRICORN products was formulated. The common design utilizes a bit structured organization with micro-program control. Hardware implementation is in TTL Gate Arrays and the complete I/O module is contained in a single board. First application will be on CHAPARRAL.

CHAPARRAL HARDWARE SIMULATOR - Hardware simulator prototypes were built and checkout initiated on these elements for the CHAPPARAL product: System Support Processor, Main Storage Unit, Disk Controller Channel and Instruction Processor Arithmetic Unit. These system elements were implemented in simulated (prototypes) hardware using a mother/daughter board configuration. The implementation technique used permits verification of the design logic prior to commitment to gate array.

FIBER OPTIC LINK - Fiber optic technology was used for the first time in Roseville in establishing a communication link between buildings 2 and 3. The link services 115 remote terminals and a remote 90/30 in building 2, at a lower cost and with higher data rates than for leased metallic circuits. In addition the fiber optic cable used is smaller and lighter than metallic and is immune to electrical interference.

CPU MONITOR IN CSF- A performance monitoring system for Central Processing Units (CPU) was developed and installed in the Roseville Computer Services Facility (CSF). The monitor system provides information which allows CSF Operations to spot bottlenecks and make adjustments for improved system productivity. Percent utilization of the CPU's in a system is monitored continuously. Utilization can be displayed graphically in real time (see photo) or plotted as a function of elapsed time.

PATENT APPLICATIONS RECORDS - Records were set in November for the number of patent applications filed at one time for a single product (12) and by an individual (9). A total of 18 patent application awards at $150 each were made on these inventions which pertain to the Cache Disk product.

{Editor's Note: Many of these patents are also displayed on the history wall.}

FY '82 Engineering Highlights:

FIRST PRODUCTS USING 64K STORAGE DEVICES - Introduction of the 64K (65,536 bit) storage device technology into Sperry Univac products was accomplished. Prototype memories were in test simultaneously for these products; System 80, Cache/Disk, 1100/63-64, DCP40, CIRRUS and CHAPARRAL. Three of these products have been announced and highlights and features of their storage applications are as follows

SYSTEM 80 - First small scale Sperry Univac computer to use the 64K storage device. Four megabyte storage module contained on one pluggable PC board (see photo). First customer delivery was in March 1982.

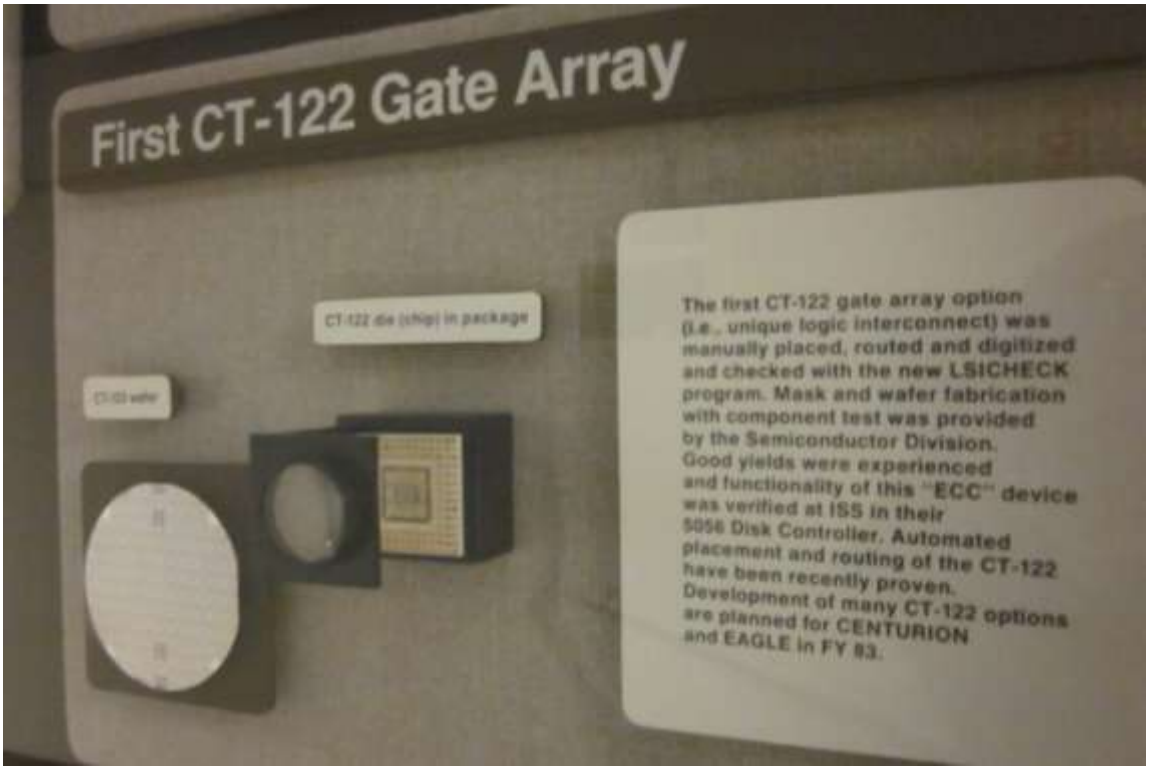
CACHE/DISK - TYPE 7053 STORAGE- With Type 5057 Controller and Disk units, provide Cache/Disk subsystem for 1100 series products.16 megabytes of storage in 36" wide cabinet with uninterruptable power supply.

1100/63-64 - First large scale Sperry Univac computer system to use the 64K device. Type 7049 Storage has capacity of 4 million words in one 36" wide cabinet. *A completely populated -Type 7049- Storage array board (Prototype) 45 bits X 131 words* and *64 K storage device with lid removed.*

CHAPARRAL SYSTEM - All Hardware Systems in Test-Build of the first complete CHAPARRAL System prototype in simulator form (one to one logic equivalent) was completed. Test of this system progressed to the point where the hardware design has been verified on the System Support Processor, Main Storage Unit, Disk/Controller Channel and the Arithmetic Section of the Instruction Processor. Prototype build in gate array logic form was initiated. Load of the diagnostic software operating system to software and further hardware testing was achieved.

EAGLE SCIENTIFIC PROCESSOR -The architectural definition and system product description were completed and design of the EAGLE processor subsystem was started. The EAGLE processor, the largest and fastest ever conceived by Univac, is a scientific processor which attaches to the CIRRUS system and utilizes high performance storage units. The EAGLE processor is capable of 133 megaflops (millions of floating point operations per second). Each high performance storage unit can interface with a maximum of two EAGLE processors

FIRST CT-122 GATE ARRAY - The first CT-122 gate array option (i.e., unique logic



interconnect) was manually placed, routed and digitized and checked with the new LSICHECK program. Mask and wafer fabrication with component test was provided by the Semiconductor Division. Good yields were experienced and functionality of this "ECC" device was verified at ISS in their 5056 Disk Controller. Automated placement and routing of the CT-122 have been recently proven. Developments of many CT-122 options are planned for CENTURION and EAGLE in FY'83.

CIRRUS PROTOTYPE SYSTEM -The CIRRUS system is a high performance extension of the 1100-Series product line. It is well along in the development process and is planned for product announcement in the next fiscal year. Major milestones achieved in FY'82: Prototype system hardware integration. Console tested on 1100/80 with System Software. In-Unit Card Test (IUCT) demonstration. IUCT is a self-contained fault detection system. Lead Main Storage Units operational in prototype system.

The CIRRUS central complex equipment incorporates many firsts for Sperry Univac products: First product use of liquid cooled High Performance Packaging in the Instruction Processor). First implementation of IUCT; The most extensive error detection and reporting of any Sperry Univac product. First use of distributed control store. First implementation of Extended Mode Architecture

1000TH 1100/60 PROCESSOR DELIVERED - On January 22, 1982 Sperry Univac delivered the 1000th 1100/60 Processor to a Twin Cities customer - Valspar. This landmark event occurred just two years after the first delivery of an 1100/60 system. Major Systems Division, Roseville Operations, designer and manufacturer of the 1100/60 is justifiably proud of the successes achieved by this product; the first Series 1100 System to ship 1000 processors. The highest delivery rate of any Series 1100 product. The first major computer system anywhere to utilize multi-microprocessor architecture.

1100/60 4X4 ANNOUNCEMENT - In December 1981 Sperry Univac announced the 3X3 and 4X4 versions of the highly successful 1100/60 system. These expanded configurations employing 3 or 4 Instruction Processors and 3 or 4 Input/Output Processors offer increased performance and availability over the current 1100/60 product. The 3X3 and $x4 systems include the new Type 7049 free-standing with 64 K MOS RAM technology and a capacity of four million words.

CENTURION SYSTEMS DEFINITION COMPLETE - Definition of the CENTURION system was completed and full scale development was initiated. The mid-range C-Series product will be an optimized balance between cost and performance in business and scientific applications.

FIRST FULLY AUTOMATED DESIGN OF GATE ARRAYS - The first fully automated gate array designs were completed. These gate array designs, to be used in the CHAPARRAL system utilized computer aided design as follows: Layout using the Computerized Gate Array Layout system (CGAL)-Automated checking of the logic versus layout and polygon rules using LSI/CHECK- Automated test list generation using CONSIM-Automated design rule spacing check using NCA software.

FIRST FIPS COMPLIANT 1100 SERIES SYSTEM SHIPPED - First deliveries were made of 1100/60 and 1100/80 Systems with input/output (I/O) channels complying with new Federal Information Processing Standards (FIPS). New I/O hardware and software features were designed to operate special tape and disk subsystems in compatible channel mode; the basis of the Federal Information Processing Standards

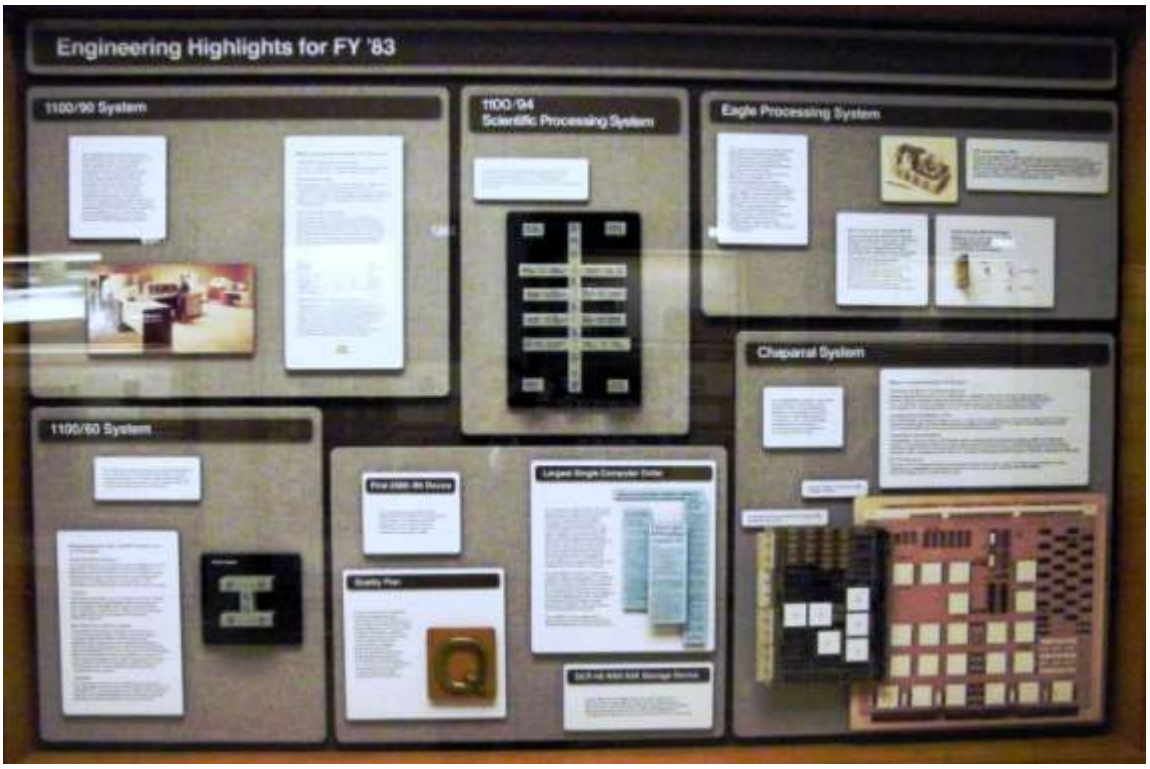
CONCURENT FAULT SIMULATOR (CONSIM) - CONSIM a Computer Aided Design system which assists logic designers in the generation of “test lists” (test information for IC devices and PC boards) was placed into production. This system takes advantage of 1100 system scan-set logic and consists of three major parts: Software to partition chips, cards and units into logic blocks, an automatic pattern generator and fault simulator which uses the generated patterns to produce a static fault test list and provides a measurement of test list quality.

FIRST DELIVERY- ARRAY PROCESSOR SUBSYSTEM - Delivery of the first 1100/80 Array Processor Subsystem (APS) occurred on January 15, 1982. The APS was installed on an 1100/84 at the Shell Oil Company in Houston, Texas, where it will be used for the processing of seismic data for oil exploration.

IN-UNIT CARD TEST (IUCT) FEASIBILITY - CIRRUS will be the first Sperry Univac product to use a new in-circuit fault location concept called IUCT. The IUCT system employs a structured design using 100% scan set and new computer aided design software (SNAP/CONSIM). Tests generated from the hardware design base (The logic equation file) can be automatically invoked by the System Support Processor to identify failed components. For select faults identification of the failing chip is achieved in less than 6 minutes average for the Instruction Processor. A demonstration of the IUCT was run successfully on the CIRRUS prototype hardware in December 1981.

COMPUTERIZED GATE ARRAY LAYOUT (CGAL) - The computerized Gate Array Layout System has been fully implemented into three unique VLSI technologies. Automated production layouts are being processed for ECL (CT-122), Schottky TTL (ST-101 and 103) and CMOS (C2G02) parts. CGAL is currently in full production at Roseville and Eagan and installed at Cupertino and Salt Lake City. The 18 Automated Layers Team is processing ST-101 and 103 gate arrays at the rate of six per week for the CHAPARRAL project using this automated process. CGAL is completing over 80% of the connections. Also the first production DSP CMOS part used 68% of the available gates and was over 88% routed by CGAL. CGAL production process flow chart is shown as are CMOS LSI plots of interconnect layers. Also DRAZO transparencies at 24X1 enlargement.

FY '83 Engineering Highlights:



1100/90 SYSTEM - The 1100/90 system emerged from its development cycle where it was known by its internal code name CIRRUS. The 110/90 is the most powerful 1100 series system developed to date by Sperry. It has a work capacity of seven million instructions/ sec per processor and real memory of up to 16 million words. Features include modularity up to a 4X4 system- four Instruction Processors (IP) and four Input/Output Processors (IOP) and virtual memory capability. Scientific processing capability of the 1100/90 can be enhanced by the addition of or two EAGLE Processing Subsystems.

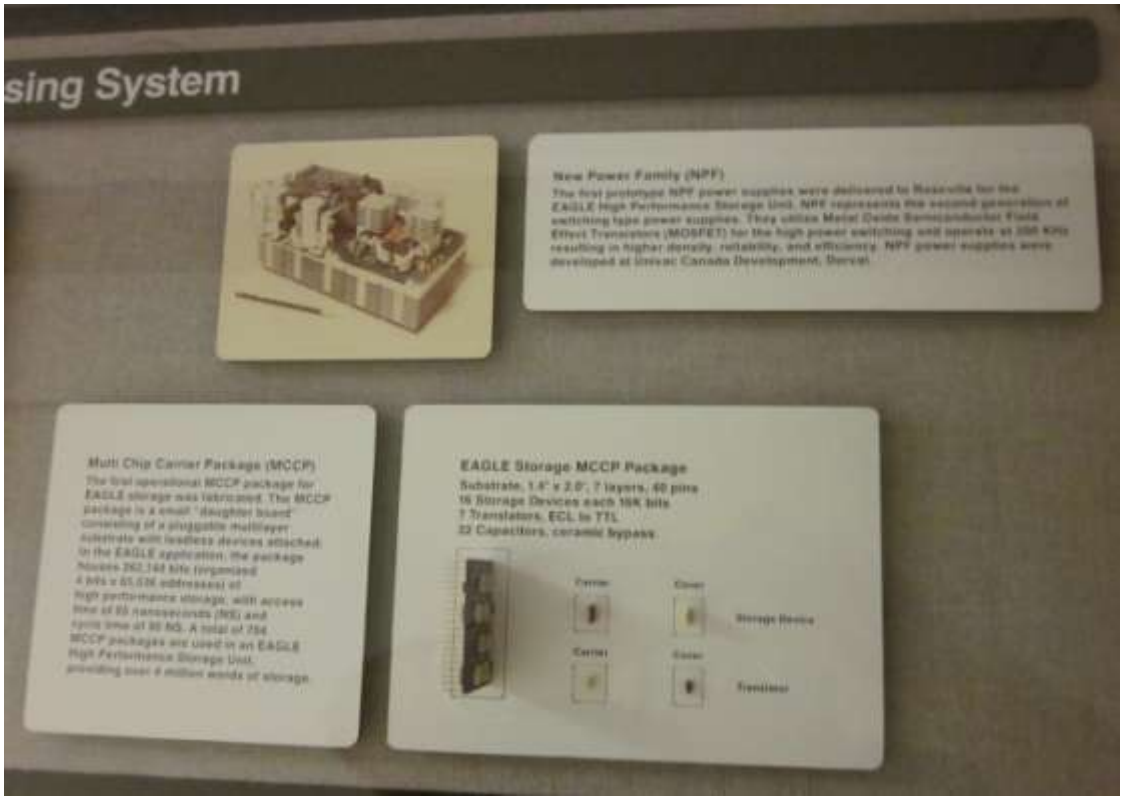
Major Milestones Achieved In Fy83 Were:

- 1100/90 Product Announcement was on July 14, 1982 at press conferences in New York and London. On December 22, 1982 an 1100/90 2X2 configuration was demonstrated using design verification software and covering the areas of system interface, system I/O loading under SIGMA (Field Maintenance) Executive control and Peripheral Test Sequence (PTS) operation.
- The 1100/90 IOP configured in a 1X1 system successfully performed a series of on-line tests to verify the design integrity of the units' modules. Thirteen separate tests were run which exercised the instruction execution, chaining functions and program error checking for the block multiplexer, the Internally Specified Index (ISI) word channel and the Externally Specified Index (ESI) word channel.
- The In Unit Card Test (IUCT), the 1100/90 maintenance system developed for field failure location to the chip level, was used to support IP checkout. IUCT has proven to be 4 to 5

times faster than conventional techniques in finding quality problems such as rework instruction errors, mis-wires, bad chips, connector problems, etc. The key advantage to IUCT is its ability to find problems without disturbing the environment: i.e. pulling cards. Gate Array Package Improvement- The gate arrays for the 1100/90 IP are packaged in a high density, high thermal performance ceramic chip carrier designed by Sperry. A package design using a tungsten-copper heat spreader material as the base was developed which is superior to previous designs in manufacturability and rework ability. This is believed to be the first use of tungsten-copper in chip carrier design.

1100/94 SCIENTIFIC PROCESSING SYSTEM - This scale model represents the maximum central processing group equipment configuration and includes four 1100/90 IP's, four 1100/90 IOP's and two EAGLE Processing Subsystems and 16 million words of storage.

EAGLE PROCESSING SYSTEM -The logical, electrical and mechanical designs of the EAGLE Processing Subsystem were completed this year and the prototype build started. The Subsystem, including the EAGLE Scientific Processor, the High Performance Storage Unit and Multiple Unit Adapter, is a specialized attached processor for the 1100/90 System. Containing 5,500 Sub nanosecond Emitter Coupled Logic (SNECL) gate arrays and 6,000 SNECL11 MSI/SSI chips in liquid cooled High Performance Packaging, an EAGLE subsystem can exercise up to 133 million floating point operations per second. The adjacent model illustrates a maximum configuration 1100/94 Scientific Processing System.



Other Major Events In FY83 Were:

Multi Chip Carrier Package (MCCP) - The first operational MCCP for EAGLE storage was fabricated. The MCCP is a small "daughter board" consisting of a pluggable multilayer substrate with leadless devices attached. In the EAGLE application, the package houses 262,144 bit (organized 4 bits X 65,536 addresses of high performance storage with access time of 65 nanoseconds (NS). A total of 704 MCCP are used in an EAGLE High Performance Storage Unit, providing over 4 million words of storage.

EAGLE Storage MCCP Package - Substrate, 1.4" x2.0", 7 layers, 40 pins, 16 Storage Devices each with 16K bits, 7 Transistors, ECL to TTL, 32 Capacitors, ceramic bypass.

New Power Family (NPF) - The first prototype NPF power supplies were delivered to Roseville for the EAGLE High Performance Storage Unit. NPF represents the second generation of switching type power supplies. They utilize Metal Oxide Semiconductor Field Effect Transistors (MOSFET) for the high power switching and operate at 200 KHz resulting in higher density, reliability and efficiency. NPF power supplies were developed at Univac Canada Development, Dorval.

CHAPARRAL SYSTEM -The CHAPARRAL System, now under development, will provide a full range of 1100 Operating System features to new-name entry level customers. CHAPARRAL will be available in one or two processor configurations, and will be price/performance competitive in the sub-1100/60 range.

Major Chaparral Accomplishments in FY83 were:

Prototype Hardware Completion and Test. System testing has started on the CHAPARRAL prototype Instruction Processor, Main Storage Unit, System Support Processor, Byte Bus Channel and Block Multiplexer Channel. P. C. assemblies are now installed in the prototype S-bus, L-bus Card including the console C.U. Workstation, C.U. Communications Line, C.U. and L-bus Adapter are also being system tested.

Prototype Storage Module in Test. The CHAPARRAL prototype storage module, 1 million words of storage on 3 P.C. boards, began test on July 6, 1982.

Storage module logic. Using 17 gate arrays of 12 logic types is contained on one P.C. board. Two storage array boards each hold 524,288 words of storage and use 64K-bit storage devices.

Integrated Communications. CHAPARRAL is the first of the 1100 Series to have communications hardware contained within the mainframe cabinet. The integrated hardware provides three communications options. The Workstation Control Unit and the Communications Control Unit, developed at Roseville, are the entry level options. An Integrated Communications Processor (ICP0, developed at Salt Lake City provides a Distributed Communications Processor capability and TELECON.

ST-100 Gate Array. The last of 127 ST-100 Series Gate Array types completed fabrication in Sperry's Egan Semiconductor Facility allowing the CHAPARRAL Instruction Processor to begin prototype checkout. The CHAPARRAL Central Complex Units use 239 Gate Arrays. *Integrated Communications Processor (ICP) installs in the L-bus. System Support Processor (SSP) installs in S-bus. Actual hardware for both shown.*

1100/60 SYSTEM - The 1100/60 product, announced and first delivered to a customer in FY80, continued to be a strong revenue producer for Sperry. After three years of market life, approximately 1,400 systems with over 1,750 processors have been shipped.

Enhancements To The 1100/60 Product Line In FY83 Were:

Dyad (1100/60-11) Product. The 1100/60 Dyad is a redesign of the 1100/60 mainframe. Removal of internal storage enables the addition of a second SIU and a second Processor in a single cabinet. Dycad uses the Type 7049 free standing storage with a capacity of 4 million words in one cabinet. It was developed on an RPQ basis for NUK local sales in Japan.

1100/64. The newest extension of the 1100/60 family was first delivered in December 1982. Using the new free standing T7049 Main Storage Unit. The system has a maximum capacity of 8 million words of storage and is configured utilizing four CPU/IOU cabinets. *System Model.*

Emulation of U-418-II on 1100/60. This project achieved the design and installation of microcode and unique software that provided a customer with the ability to load and execute existing 41811 programs on the 1100/60.

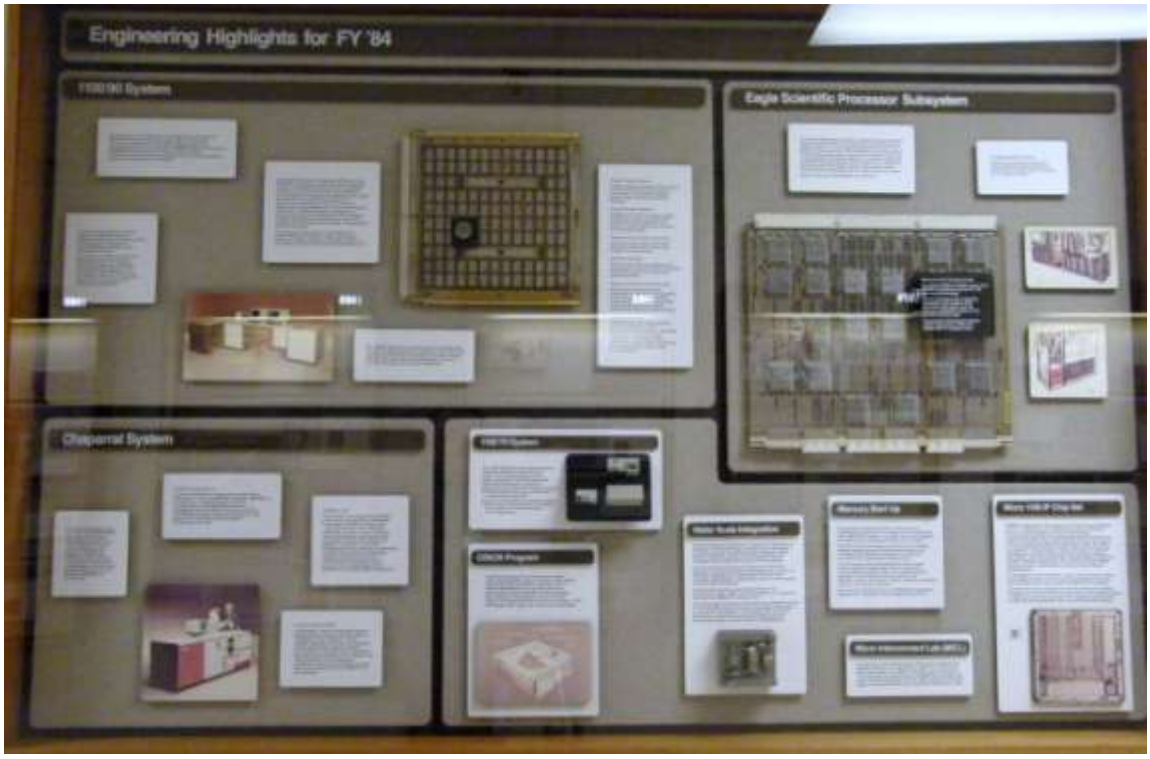
FIRST 256K-BIT DEVICE. First engineering samples of the 256K dynamic random access memory were tested. This device has the capacity to store 262,144 bits of information and will be used in products introduced in1985

QUALITY PLAN. A plan for Roseville Hardware Product Operations was developed with the objective of improving the quality off our work, thus helping to insure the quality of Sperry products. The Plan outlines areas in which quality improvement efforts will concentrate, including: Quality awareness, Documentation processes and Employee participation. The Quality Circles Program in Hardware Product Operations was expanded to seventeen Circles with 135 people participating during FY83.

LARGEST SINGLE COMPUTER ORDER. On January 27, 1983 the U. S. Air Force announced that Sperry had received a $476.2 million contract to supply computer systems for Air Force installations around the world. The contract calls for replacement of 287 older, obsolete computers with 150 Sperry 1100/60 large scale systems with more than 20,000 communications terminals. Over the next 29 months the new technology advanced Sperry computers will be installed at all major Air Force installations around the world, beginning in May with Langley Air Force Base in Virginia. The new Sperry systems, replacing a variety of second –generation computers installed in the mid-1960's, will support Air Force Combat missions requirements for handling aircraft parts inventories and maintenance operations throughout the world .Additionally, the 1100/60's will perform a wide range of base personnel, financial, Civil engineering and administrative functions. The 1100/60 central system was developed by and is manufactured by Roseville Hardware Product Operations. *The actual newspaper articles are shown.*

DCP/40 WITH 64K STORAGE DEVICES. In July 1982, first customer delivery was made of the DCP-40 product with 64K storage devices replacing the 16K devices in main storage. Storage capacity of the product was increased by a factor of four (from 512 kilobytes to 2 megabytes) using the same size and quantity of array boards.

FY ’84 Engineering Highlights:



1100/90 SYSTEM. Development of advanced technology system progressed toward first customer delivery in April 1984. In complexity as well as in performance, the 1100/90 System is the most challenging product ever launched at Sperry Roseville Operations. Highlights of the past year, as well as unique features of the System and innovative techniques used in the development process are described below.

The Performance Monitor Feature F4089 is an attachment to the Instruction Processor (IP) that provides for the connection of external instrumentation to monitor up to 160 points of IP logic. This feature is required to decouple the probe points from the high performance logic, to amplify the attenuated probe signals, to drive the external instrumentation, and to provide an RFI secure connection block for the attachment of the external instrumentation.

The High Performance Packaging (HPP) used in the 1100/90 IP is extremely dense and utilizes multilayer printed circuit boards. Rework of these assemblies involves very small wires which must be bonded to a ground plane. Changes must, therefore be "right" the first time as it would not be practical to remove and reinstall them later. To assure that these severe requirements were met a new program called (CIVIL) CIRRUS Interactive Validation of Interconnect Logic) was developed. CIVIL validates changes against logic and wiring rules, generates equations and interconnect file updates and generates rework instructions.

The 1100/90 Operator's Console uses the UTS-60C Color Terminal to display operator information.

- Design Change Initiated- Design Engineer determines how change is to be made and notifies Validators (see step 2) via automated logging system which records all problems and fixes.
- Design Change Validation- Validators use CIVIL to assure change compliance to logic and wiring rules. Enables one-time installation and recovery. Result: Shortened schedule and improved quality.
- Computer Aided Rework Generation- CIVIL generates rework instructions errors and shortens turnaround time. Interactive Routing- Routing instructions are generated by the Computer Aided Net Online Evaluation (CANOE) program on an interactive graphics terminal.
- Rework Instruction Preparatory (RIP) - RIP formats and stores rework instructions in MAPPER, thus available to all work centers simultaneously. Output hardcopy is in standard format and becomes part of the official Engineering Information Release (EIR).
- Rework Installation- The final step in the rework process is actual installation of the specified changes in the P.C. assembly. The closely controlled change verification and printed rework instructions greatly reduce the chance of error and result in high quality P.C. assemblies.

CHAPARRAL SYSTEM - The first CHAPARRAL product was announced on November 7, 1983: the MAPPER 10 System. The MAPPER 10 is a specially configured system oriented to applications using MAPPER software. In a subsequent announcement, the general purpose CHAPPARAL product, designated System 11, was announced. First delivery is scheduled for first quarter FY85. Products developed under the code name CHAPARRAL were introduced to the marketplace during FY84. This product line's basic price/performance are below the 1100/60 and 1100/70,but with options including a dual processor configuration, a broad range of applications is covered.

Program highlights for FY84- Customer Set Up (CSU)

The CHAPARRAL is the first Roseville system designated for Customer Set Up and installation by customer. This is possible because of its ease of installation and its high quality, reliable hardware and software. A complete set of installation manuals is being provided for customer. CSU avoids the cost of sending an installation crew to each customer location and is advantageous to both Sperry and the customer.

EAGLE SCIENTIFIC PROCESSOR SUBSYSTEM - The EAGLE Subsystem consists of a special purpose Scientific Vector Processor (VSP) and a High Performance Storage Unit (HPSU).Either one or two EAGLE Subsystems with one to four HPSU's may be used in an 1100/90 System for very high speed scientific processing. When more than one HPSU is used, one or two Multiple Unit Adapters (MUA) are required. A maximum Scientific Processing System would consist of an 1100/90 4X4, four instruction processors and four Input/Output Units), and two EAGLE Subsystems with 16 million words of storage. Major milestones accomplished in FY84 were the Prototype EAGLE Hardware design and prototype construction completion and test initiated on SVP and the HPSU which are shown in the adjacent photos. First use of CT-122 Gate Arrays. The EAGLE HPSU and MUA are the first Sperry products to use the CT-122 gate array technology. The CT-122 gate array is 10K ECL compatible and contains 1500 equivalent logic gates, with an average propagation delay of 1.25 nanoseconds per gate.

1100/70 SYSTEM - The 1100/70 System was announced and customer deliveries were started in FY84 The 1100/70 is based on the highly successful 1100/60 System with improved performance, enhanced appearance and extended storage capacity. Floating Point instruction

performance is improved by 25% to 30%. A new console table is used (see model). Maximum storage capacity is increased from 2 million to 8 million words in any configuration.

ORION PROGRAM - Development of the first 1100 microcomputer -code named ORION- began in August 1981. ORION will use the 1100 custom VLSI chip set and the DSP-20 (MAPPER) to bring 1100 mainframe performance and functionality to microcomputer size and costs. The program is in the start-up phase. The adjacent sketch shows the proposed "CPU" with integral disk, tape and random access storage.

MERCURY START UP - During the first quarter of FY84 a task team was established to select the technology for the components of the MERCURY System. In parallel plans were made for the staffing and a dedicated location for the project. The wafer scale technology selected for the processor design required teams of technical specialists to be in residence at TRILOGY Corporation in California as a part of the technology transfer project. The occupancy of the dedicated Earle Brown location started in September with the installation of the Amdahl Computer center. The staffing build up included a new automatic design group for the TRILOGY unique CAD system. And an extensive recruiting drive for logic design personnel. As a result of the FY84 effort the MERCURY project was positioned for the start of detail design during FY 85.

MICRO 1100 IP CHIP SET - SPERRY Corporation's first custom VLSI Chip Set was designed in FY84, implementing an DIDI Series Instruction Processor. Four of six chips implement a basic TYDI processor. The Extended Instruction Set and Multiply/Divide Floating Point optional accelerator chips combined with the basic set support a unit processing performance comparable to more than 200% of a System 11 unit processor. The six chip types are typically packaged in a common 224-pin Grid Array package. The number of active transistors per chip (package) ranges from 75,000 to 165,000: implemented via 1.25 micron. N-well CMOS Structured Custom, Semi-Custom and true Custom Design.

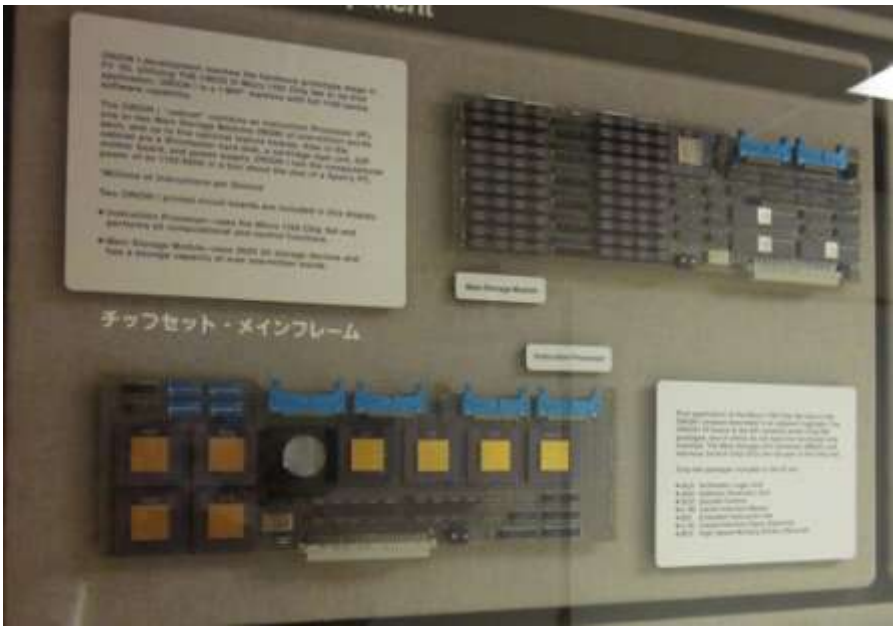
MICRO INTERCONNECT LAB (MICL) - Construction of the Semiconductor Operations Headquarters building in Eagan was expanded to include four bays for the Micro Interconnect Lab (MICL). The MICL Lab is working on next generation interconnects for the MERCURY package and other multichip packaging schemes. MICL personnel moved to Eagan in July and the Lab was completed in September 1983.

WAFER SCALE INTEGRATION - TRIOLOGY Systems Corporation of Cupertino, California is a developer in the technology of designing and fabricating computer products using Wafer Scale Integration (WSI). Under an option to license, this technology is being evaluated and considered for use in future products. In FY84 teams of technical specialists from Roseville Operations and Semiconductor Operations were resident at TRILOGY, studying and evaluating the TRILOGY WSI Computer Aided Design (CAD) System and the wafer design and fabrication techniques. A dedicated computer center was installed at the Earle Brown Tower (EBT) location to further the evaluation and serve the MERCURY design effort. The technical evaluation is planned to be completed during FY85. Utilization of the TRILOGY technology is dependent on satisfactory completion of evaluation and exercise of the Option to obtain the License and rights to use the technology.

FY '85 Engineering Highlights**:**

MICRO 1100 DEVELOPMENT - ORION 1 Development reached the hardware prototype stage in FY85, utilizing the CMOS 111 Micro 1100 Chip Set in its first application. ORION 1 is a 1-MIP (millions of instructions per second) machine with full 1100 series software capability. The ORION 1 "cabinet" contains an instruction processor (IP), one or two Main Storage

Modules (MSM) of one million words each and up to five optional test feature boards. Also in the cabinet is a Winchester hard disk, a cartridge tape unit, and IOP mother board and power supply. Orion 1 has the computational power of an 1100/60 H2 in box about the size of a Sperry PC. The instruction processor uses the Micro 1100 Chip Set and performs all computational and control functions. The Main Storage Module uses 262K bit storage devices and has a storage capacity of over 1 million words.



First application of the Micro 1100 Chip Set was in the ORION1 product described in an adjacent highlight. The ORION 1 IP board at the left contains seven Chip-Set packages, two of which do not have the functional chip installed. The Main Storage Unit Controller (MSUC) and Interface Controller Chip (ICC) are not part of the Chip-Set. Chip-Set packages included in the IP are: ALU- Arithmetic Logic Unit, AGU- Address Generator Unit, DCD- Decode Control, CIM- Cache Interface Master, EIS- Extended Instruction Set, CIS- Cache Interface Slave(Optional), and M/D- High Speed Multiply /Divide (Optional).

SOFTWARE DEVELOPMENT - The SX 1100 1R1 system, delivered on January 18, 1985, was the first Sperry UNIX product to reach the marketplace. This system brings the rich functionality on UNIX to the 1100 series customer base. Sperry was first major computer manufacturer to announce and deliver UNIX on personal computer through mainframe products. *UNIX is a trademark of AT&T Bell Laboratories.*

The release of CS1100 RTE marks the first availability of a high volume communications simulation driver which executes on a standard DCP (Distribute Communications Processor) front end processor. RTE satisfies a broad range of terminal communication simulation needs- from function testing of software applications to capacity testing of total computer systems. This software tool introduces two major advancements: 10 Elimination of the need for a separate mainframe (Series 1100 system) to serve as a driving system, and 2) Provision for truly high volume simulation environments.

Software CSU capability was developed to enable the customer to rapidly install 1100 System software without Sperry assistance. With the CSU process, all software products for a system are pre-installed on one tape enabling the customer to "set-up" the system in fraction of the time previously required. The ultimate goal of this development process is "instant" installation, i.e., minutes instead of hours, or even days, as was once the case.

Three general purpose PC-to-1100 mainframe link software products were developed in FY'85 using deployment prototyping methods. These products were among the first developed by Sperry to integrate the mainframe and the desk-top Personal Computer. Employing an innovative prototype development method using a team consisting of programmers, writers and system testers and incorporating ongoing process improvement, these products were developed quickly and with very high quality.

INTEGRATED SCIENTIFIC PROCESSOR (ISP) SYSTEM - The ISP project, known internally as the EAGLE project, completed several major milestones aimed at scheduled product announcement in early FY'86. The ISP system which operates as an adjunct to the 1100/90 system with high performance storage units, provides super-computer performance in a general purpose computer system.

Significant Milestones Achieved In FY'85 Were:

ISP Hardware Units Demonstrated, July 1984. ISP and 1100/90 Hardware Systems Functionality Demonstration, January 1985. Extended Mode software releases delivered to Shell Oil Company in December 1984 and March 1985.The first application of the ISP will be in Seismic data processing (oil exploration). Additional applications are anticipated in satellite data reduction, reservoir modeling, weather forecasting and molecular engineering.

MAPPER - The Personal MAPPER System was the star of the preannouncement debuts at the Spring USE and SUAE user conferences. This product packages a specially adapted version of the MAPPER 5 software on a PC feature board. This board contains a powerful Motorola 68010 processor with 512 bytes of memory. The Personal MAPPER board brings the power and flexibility of the MAPPER system to Sperry PC and IBM XT users. The Personal MAPPER System is in functional test and will be available for shipment to customers in early FY'86. The Sperry MAPPER 5 system completed system test on September 15, 1984. By the end of FY'85 over 700 units had been shipped to Sperry and customer sites. The MAPPER 5 system is a completely new desk-top implementation of the MAPPER system. Based on the Motorola 68010 micro-processor, MAPPER5 supports 8 concurrent users and 199 million characters of disk storage.

1100/90-culminating the six years of development, the first 1100/90 System were shipped in April 1984 to Bell Communications Research, Piscataway, New Jersey and to Yamaichi Securities Co. in Tokyo, Japan. In October of 1984, the first 1100/94's four Instruction Processors) were shipped to Shell Oil Company, Houston, Texas and to Yamaichi Securities, Tokyo. A total of 160 Instruction Processors (IP) were shipped in FY'85. The 1100/90 system is

the most powerful in the 1100 Series. Performance ranges from 7 MIPS (millions of instructions per second) for the1100/91 to 26 MIPS for the 1100/94. The 1100/90 has technology advancements in architecture, security, availability, reliability maintainability and install ability. One example of the enhancements present in the 1100/90 is the cable labeling system illustrated in the adjacent photo. The large number of cables required to interconnect units in a system of this size is a major factor in installation time. For the 1100/90, a book of color coded labels is provided to pre-mark cable origin and destination. The labeling system significantly reduces the time and cost of installation.

DPC PACKAGING - The DPC (Dense Printed Circuit) packaging method has been selected for use in the MERCURY project. The DPC packaging approach employs three different sizes of integrated circuit packages, as shown in the adjacent photo of a DPC module mockup. The larger Package size will contain gate arrays, which will be used in the data path and time-critical areas with lower risk of changing. The medium size package will contain generic gate arrays used for the general purpose control latches. The Small Scale Integration (SSI) logic will use the small package and will be used for the Ram's and random control logic which has a higher risk of changing. The printed circuit board will then bear the burden of the IC interconnect and most of the changes will occur at that level.

LUMIN - The LUMIN (Local Univac Message Interconnect Network) architecture specification, Revision P2 was completed in December 1984. LUMIN is a message-based architecture, which provides efficient and flexible means for transmitting data and control information between nodes (stations) in a ring network. The adjacent network diagram illustrates the types of system components, which may be connected by LUMIN. A physically simple bit-serial data path based on fiber-optic technology permits very high-speed (100 million bits per second) transmission between nodes up to 1 kilometer apart.

HCADS - (Hierarchical Computer Aided Design System) developed to enhance designer productivity and improve product quality, was introduced in January 1985. The system based on an open architecture design utilizes the latest data management techniques to support hierarchical design concepts. The system offers new logic design tools for hardware design descriptions, verification, and design data management.

FIBER OPTICS - Fiber Optics technology, as planned for use in the LUMIN ring network, is a major advance in data transmission capability over the presently used coaxial cables in the adjacent photo. The two single-fiber optical cables on the right have the same data capacity (100 million bits per second) as the eight coaxial cables on the left. In addition to the physical size difference, the optical cables are more rugged, are immune from and produce no outside electrical interference, cannot practically be wire-tapped and can operate at a distance of up to one kilometer without amplification.

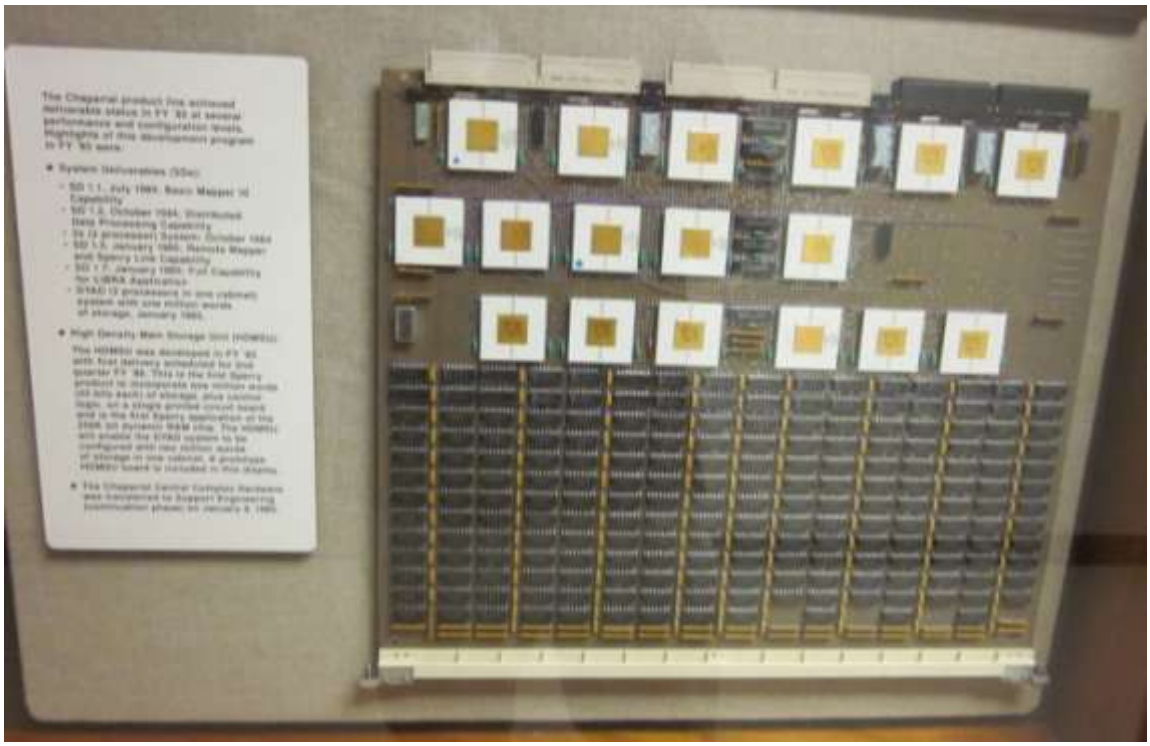
MULTI USAGE I/O - Multi Usage I/O Processor elements that can be used in several new products, e.g. MERCURY and LIBERTY, are being developed. Modularity is provided by a

bus structure concept that allows elements of various types to be added as required. Peripheral subsystem interfaces to be supported include FIPS-PUB 60-2 Intelligent Peripheral Interface (IPI) and word channels.

CHAPARRAL SYSTEM -The CHAPARRAL product line achieved deliverable status in FY'85 at several performance and configuration levels. Highlights of this development program in FY'85 were:

- System deliverables (SD's) - SD1.1, July 1984, Basic MAPPER 10 Capability- SD1.2, October 1984, Distributed Data Processing Capability- 2X (2 processor) System; October 1984- SD 1.5, January 1985; Remote Mapper and Sperry Link Capability- SD1.7, January 1985; Full Capability for LIBRA Application- DYAD (2 processors in one cabinet) system with 1 million words of storage, January 1985.
- High Density Main Storage Unit (HDMSU) was developed in FY'85 with first delivery scheduled for 2nd quarter FY'86. This is the first Sperry product to incorporate one million words (43 bits each) of storage plus control logic on a single printed circuit board and is the first Sperry application of the 256K bit dynamic RAM chip. The HDMSU will enable the DYAD system to be configured with two million words of storage in one cabinet.

A prototype HDMSU board is included in this display with 17 VLSI and 208 DRAM memories (4916750).



- The CHAPARRAL Central Complex Hardware was transferred to Support Engineering (continuation phase) on January 9, 1985.

ACKNOWLEDGEMENTS

During 60+ years; computer technologies have evolved from vacuum tube logic through transistors, to integrated circuits with just a few single gates to over a half million equivalent gates in a device. We, the retirees of the ERA to UNISYS corporate transitions have been involved in all aspects of the technologies growth. It was very exciting and rewarding to be involved and I hope this paper has given the readers an overview of some of the Sperry to UNISYS technologies in computer history.

Bernard N. "Mike" Svendsen.

Author

I graduated in 1959 from the University of Minnesota with a Bachelor of Science degree in Electrical Engineering. I had asked my uncle (Commander Edward C. Svendsen) if he had any thoughts about the electronics industry and where I might go to work. His comment was brief: "well, UNIVAC is doing some interesting things with computers". UNIVAC was close to home so I joined in Aug '59. The semiconductor industry was in its infancy then and the majority of my 25 years at Univac were involved in semiconductor specification, design, evaluation, testing, quality, failures, cost, availability and manufacturing at our suppliers and at our in-house facility. You might say we matured together.

I worked at all of the plants in the Twin Cities and in many disciplines - Electrical Engineering, Reliability, Test, Procurement, Quality, Production, Quality Assurance, Operations Management, Bipolar Operations and the Semiconductor Control Facility. I was a member on Sperry's Corporate Councils on Semiconductors, Standardization and Procurement.

Editor

Editor of these papers is Lowell A. Benson, BEE 1966 - U of MN. Mr. Benson was a UNIVAC 1960 to UNISYS 1994 employee.

Lowell took the cover, shadow box, and hallway photos. Mike took the detail snapshots.

Our thanks to Richard Petschauer and Harry Smuda for the shadow box creations!