R. A. Erdrich, 3rd Experiences Article

by Richard A. Erdrich 'Dick'
Editing by John Skonnord, formatted by Lowell Benson.

INTRODUCTION

Mr. Erdrich was employed by UNIVAC, Sperry, Unisys Defense Systems, and Lockheed Martin in the Twin Cities for 47 years! After the Legacy Committee was formed in late 2005, retirees and employees were asked to write brief career summaries. There was absolutely nothing brief about a 47-year career, so Dick asked John Skonnord of Lockheed Martin {Publications & Design Services} to assist in putting together stories of his almost five decades of computer work history.

In December 2024, Dick gave Lowell a disc containing 17 stories along with text sheets and photographs – we've decided to post them in three segments as shown in this Table of Contents. I, Lowell, feel quite fortunate to have been directly associated with him during several of his 16-Bit Computer Stories.

Contents

Formatted for the Legacy Anthology with Microsoft Word.

In addition to these specific career stories, Dick has contributed items to the Legacy Anthology chapter 44, Interfaces; chapter 51, 24-bit Computers; chapter 52, 32-bit CPUs; chapter 54, 16bit Computers; chapter 57, AF computers; and Our Stories posted June 2010, 200 Nanosecond Memory edited by Lowell Benson with text inputs from Curt Hogenson, **Dick Erdrich**, Don Mager, Ken Pearson, et al..

1.0 30-BIT COMPUTER STORIES

Posted for February 2025; First of a trilogy of Dick Erdrich's 47-years with the Legacy companies focuses on his 30-bit computer experiences..

2.0 16-BIT COMPUTER STORIES

Posted for March 2025; Second of a trilogy of Dick Erdrich's 47-years with our Legacy companies focusing on his 16-bit computer experiences..

3.0 ADVANCED DEVELOPMENTS

3.1 Emulation Test Vehicle-1 (ETV)

This is the box that started off as the Advanced Test Device (ATD) and ended up as Emulation Test Vehicle 1(ETV-1).

Gloria Featherstone is looking with awe at the Hand-Held Maintenance panel which was developed under IRAD[1] money at the same time as we were doing the initial design of the ATD and ETV-1. I believe that Gloria worked in Integrated Logistics Support and the reason I knew her well was that I had coached her son in our local athletic association football program.

The "getting to" this point in time is a long story with some interesting facets but I will try to explain the next series of pictures from the standpoint of one that was there from beginning to end.

The first awareness I had of a need to update the Poseidon Central Navigation Computer (CNC), or CP-890, occurred in 1977 when Ray Dombeck and I were invited to visit Sperry System Management (SSM) at Great Neck, NY. We spent one very long day in a smoke-filled room where the first half of the day was spent bringing us up to speed on the Improved Accuracy Program and the second half was spent by me at a blackboard explaining how we could do the job.

The program was being run out of the Special Projects Office, SP-24, in Washington DC. SSM was the system management contractor and UNIVAC built the existing navigation computer. The relationship between SP-24 and UNIVAC engineering was about as good as it gets. We were always up front with them, even when it hurt, and they appreciated it. Tom Brahmey had been a systems engineer during the CNC project with more operational experience afloat than anyone I could think of. He was now the head man and I'm sure that our selection to be a part of this effort was his decision. One must remember that the original navigation computer for the Polaris program had been built by SSM and, even though our CNC design was superior in every way, they always felt that it was their charter to design the computer.

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[1] Reference item 3 on page 12 of https://vipclubmn.org/PeopleDocImg/Vol1Book01.pdf.

The Improved Accuracy Program would employ Correlation Sonar to measure speed and direction over the ocean bottom and an Electrostatically Suspended Gyro Navigator (ESGN) to measure ship movement. The Correlation Sonar data needed heavy signal processing to be usable and the ESGN data needed to be processed prior to being used by the software navigator.

An aside here, skipping forward 25 years; the latest proposals from SSM to update the Trident Navigation computers, currently Memory Processors, propose COTS (Commercial Off The Shelf) systems that are not Navy Standard AN/UYQ-70's, to be built by SSM. They have again demonstrated their political agility in bypassing any requirement to use Navy standard equipment. This was supported by SP-24 which has always had the desire and the clout to go their own way.

A major problem at the time was a proclamation by Congress that no further military computers would be developed. This was driven by the political power of the commercial computer makers, primarily DEC, which was scaling up their minicomputer range and trying to sell what we now know as COTS into the military mainframe market. The method we would use to develop the needed capability was to do the design in stages with the premise being that we were designing test equipment. A CNC was deployed in the Plant 1 test area for the purpose of testing and selling the I/O Buffer which we built as a part of the Poseidon Navigation System. The plan was to use this computer at a depot as a module tester, using the MTAG (Module Test Adapter Group) that I had designed following the CNC production start, and replace it with an emulator to be known as the Advanced Test Device. The ATD would be a partial emulation of the existing CNC and provide enough functionality to execute the buffer test software.

This plan was followed, and we designed the ATD using a Micro Programmable Controller (MPC) that was based on an updated UYK-20 design. We had to provide 30-bit data paths for the emulation so two of the 16-bit MPC modules were daisy-chained together with the extra 2-bits truncated.

Picture 12B (right) shows the interior of the cabinet. We needed to design a couple of Emulation Adapter modules to support the MPC but most of the execution was done in microcode.

One problem area was the number of interconnects needed between the two MPC modules. The two module connectors only provided 200 connector pins and, after accounting

for power and ground connections, left me with an unworkable design. My solution was the infamous "Over-the Top" connections. The center chassis shows the flat grey cables that were used to connect the two MPC modules together, of course, removing one module meant removing both modules. And as far as extending one of the modules, forget it! Nevertheless, we managed to get it running and demonstrated it, on schedule, in 1978.

The ETV-1 contract was awarded shortly after the ATD demo and we all kept working the "drop shift." What that means is that you work 'til you drop. What we needed to do during this effort was to complete the design and checkout of the so-called Type I instructions, everything below 77 octal, and incorporate the cache memory. It would take a lot of convincing and testing before either SSM or SP-24 would believe that cache memories could really work. I explained the theory several times and they always walked away shaking their heads. It wasn't until they were able to instrument their operational software that they were able to document a cache hit rate of >98%. The last three cards on the right of the middle tray is the cache memory. This was the first design of a Cache Memory in our division and for the military and was very near the earliest of any commercial computer.

We demonstrated ETV-1 either late in 1978 or early in 1979. The ETV-2 contract was then awarded now that we had proven that we really could emulate earlier hardware. It was shipped to SSM where it was used for many years to develop software for the Navigation Subsystem.

3.2 Emulation Test Vehicle-2

ETV-2 was a full emulation of the CP-890. It was a logical follow-on to ETV-1 and finished the emulation design of the type II instructions. It was also packaged in a CP-890 type cabinet and could very well have replaced the CP-890. It was about 3 times faster and had twice as much memory. It did not, however, provide the signal processing functions necessary to support the Improved Accuracy Program. We completed this in early 1980 and spent the summer writing the Memory Processor proposal. ETV-2 was shipped to SSM where they were able to document the cache memory performance.

Picture 13A (right) shows the closed cabinet with the hand-held maintenance panel mounted in its storage bracket. The hand-held maintenance panel concept had a short life after a Navy Officer commented that it looked too much like a hammer and some white hat would surely use it as one.

Picture 13B (left) shows the open cabinet with chassis trays and modules. The I/O chassis is on top, the processor chassis is second from the bottom, and the Memory chassis is on the bottom. The last three cards on the right that come out to the edge of the processor tray is the cache memory.

Picture 13C (below) shows a close-up of the Hand-Held Maintenance Panel. It was controlled by a 6502 4-bit microprocessor. Even though it was never fielded as shown, its circuitry found its way into all our succeeding processors including the Memory Processor, the UYK-43 and 44, and the B-2 ACC. This was an IRAD program that was worthwhile doing and helped us in making our schedules.
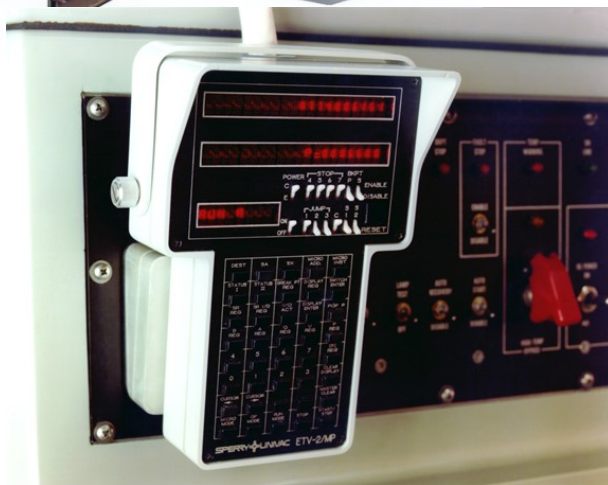
Picture 13D (right) shows the logic chassis swung out. Notice two things: the flat cables interconnecting the chassis trays, and the depth of the chassis. The decision to use flat cables for this installation rather than to build one big back panel proved to be a workable concept based to some extent on the success we had with the Over-the-

Top cables on ETV-1, In fact, the production Memory Processor back panels were connected in the same way.

The depth of the chassis was dictated by the need to use a wire-wrap design for some of the modules. At that time, we were using a 6"X9" dimension for a printed wire form factor but for wire-wrap it needed to be extended to 9"X9". This difference is noticeable in picture 13B, page 5 above.

Picture 13E (left) shows the cabinet top with 120 pin I/O connectors and the cabinet back with rear access panel.

Picture 13F (below) shows the Memory Array Module. All the RAMs shown in gold were prototype parts but performed well. This module went through layout and was built as a 6"X9" multi-layer Printed Wiring Board (PWB).
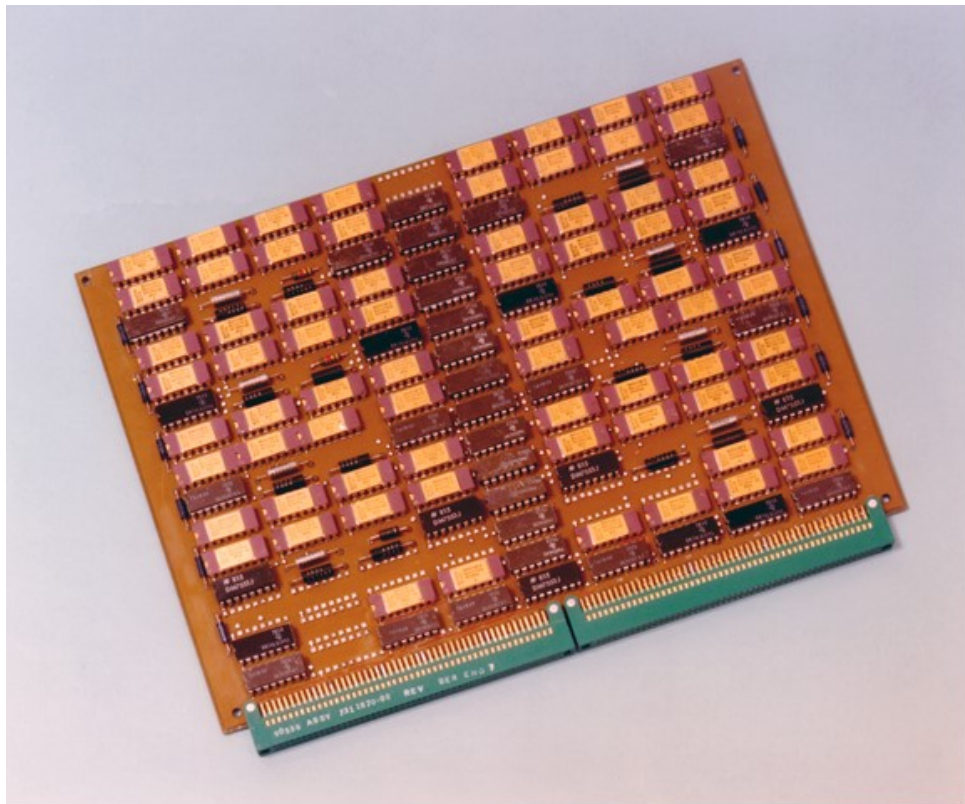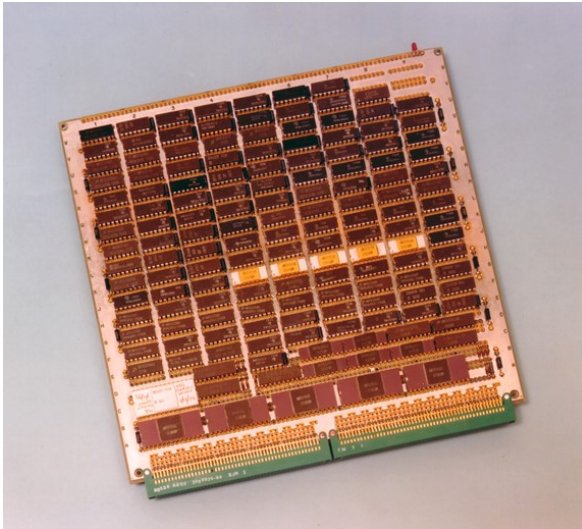
Picture   13G
(right) is the wire-wrap side of one of the
emulate modules. These boards were
entirely machine wrapped.
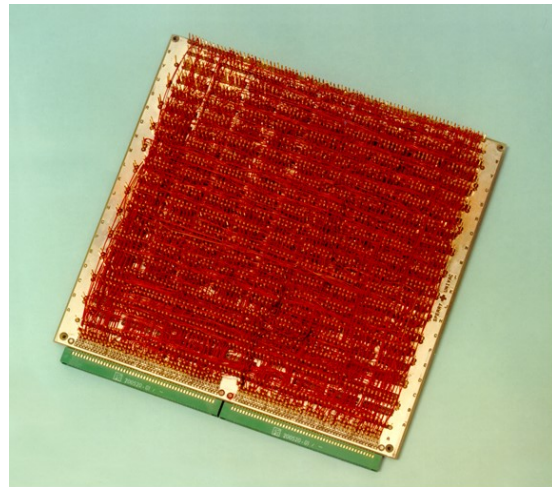
Picture 13H (below) shows the front side
of the 13G previous wire-wrap module.

Picture 13I (below) is an I/O adapter
module. i.e. Mil-Std-1397 type B. To change
I/O interfaces the adapter modules were
replaced with the appropriate one.   This
board also went through the layout process,
but was not nearly as successful as the earlier
PWB.   Note the 30-gauge rework wire
running between the chips on the left side.
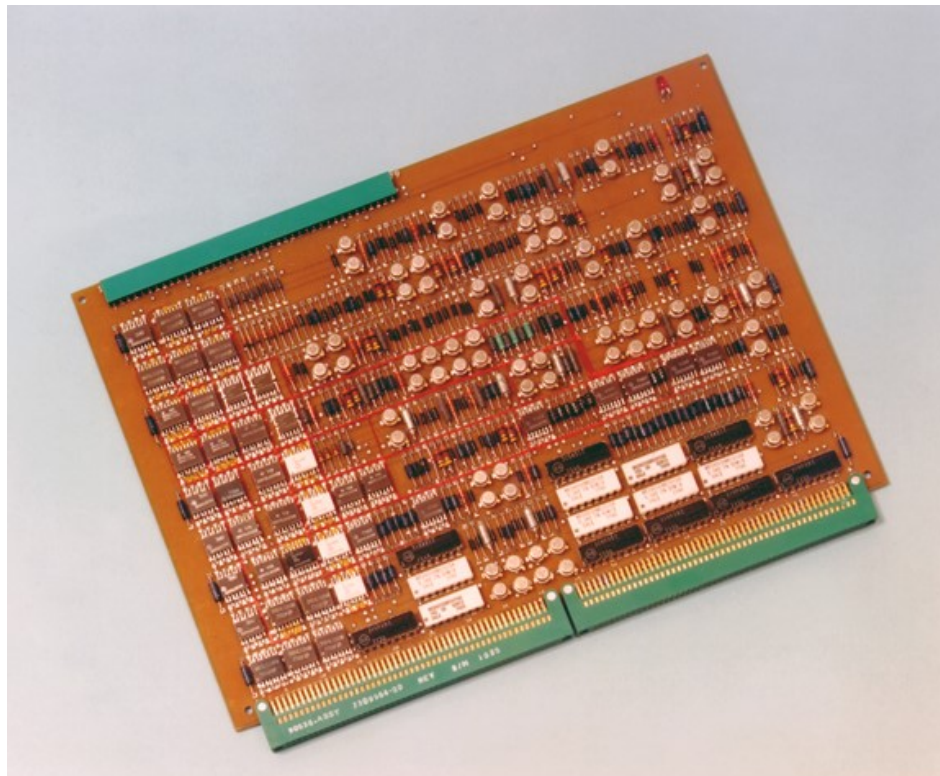
3.3 Memory Processor

The Memory Processor was the culmination of all the effort starting with ATD. It started off as an ETV-2 with added processing capabilities, principally a 32-bit mode, but evolved into a new computer architecture. See https://vipclubmn.org/cp32bit.html#MemProcessor for more information about this development.

Following the delivery of ETV-2 the powers that are in Washington decided that this should be a competitive contract. The way I understand it, an RFQ issued to perform this job did not draw any interested or qualified bidders and the Navy, already in bed with CDC on the AYK-14 computer, paid them $300k to write a competing proposal. Of course, we won the job for the same reason that everything we bid on the AYK-14 program we lost. The navy wasn't going to let us play in CDC's back yard and they weren't going to play in ours. Once the contract was signed things changed fast.

We scrapped the existing 30-bit architecture in favor of the never-defined 32-bit architecture and started defining the signal processing functions needed for the Improved Accuracy Program. I worked for 5 months defining the architecture and instruction set. When finished I had a Multiple General Register architecture with one instruction context switching (these were interrupt driven systems) and a complete set of trigonometric and complex equation functions in addition to all the normal integer and Floating arithmetic and logical operations. The indexing capabilities allowed iterative matrix operations to be interrupted and restarted and the operand address generation was pipelined beneath currently executing instructions. The address generation was designed to support ADA-generated object code and its propensity to generate pointers into arrays of pointers. There has never, to my knowledge, been another processor designed that performs these macro functions. About two weeks after completing the architecture and getting the go ahead from SSM to start design I suffered an appendix attack and was out for a month recovering from a severely run-down condition. Who says the job doesn't take it out of you?

The Memory Processor was probably the single most successful project of any size done at SPERRY UNIVAC. We met the schedule (23 months for a new computer architecture and software), met the budget, and met all of the requirements. I think we also made the maximum incentive on all the production units delivered. The Navy skipped a step in the production sequence because the EDMs performed so well they bypassed pre-production and went right into production.

Picture 14A (right) shows the closed cabinet. This series of pictures is of an EDM but the change to production was virtually undetectable.

Picture 14B (right) shows the Maintenance Panel access door open. What is shown are two maintenance panels, one for each processor. Provisions were required in the original proposal for expanded capability. While firming up the definition for the new architecture SSM interpreted this to mean a second processor. It caused me some minor problems, but I was able to connect both processors to the I/O and Memory chassis and each other. The memory wasn't much of a problem because the large caches kept the memory bandwidth to a crawl and with some of the I/O channels still running NTDS Slow I/O bandwidth would never be a problem.

Picture 14C (below) shows the two identical Maintenance Panels.

Picture 14D (below) shows the inside of the cabinet. The lower housing on the inside of the door contains a high voltage nickel-cadmium battery pack. During the initial discussions with SSM in the smoke-filled room the issue of parking the ESGN gyro came up. The Electrostatically Suspended Gyro Navigator has a small sphere in an evacuated chamber spun up and levitated electrostatically. The computer would be required to de-spin and park the sphere during normal shutdown and in the event of power failure. The ESGN power would be backed up by a battery. I was asked how we could do this with the computer. My answer was that I would put a "Die Hard" in the bottom. This drew a big laugh at the time but when the production models shipped there was a bank of batteries in the door.

When power was lost the computer would run for 5 minutes and then shut down the logic. The DRAM memory would be held up for an additional 25 minutes.

Picture 14E (left) shows the chassis tray doors open. The I/O chassis is on top, Processor 1 is right below it, Processor 2 is on the bottom, and memory is in between. At the time this box was being delivered it contained a massive amount of memory in comparison to both military and commercial computers. The processor could address 16 million words (64Mbytes) and held 4.096 million words plus syndrome bits for error detection and correction on the 16 memory modules shown in the memory chassis. The cache memory was also very large, probably one of the largest around, containing 64 thousand words (256Kbytes). Most commercial cache memories held only 256 bytes!

https://vipclubmn.org/cp32bit.html#MemProcessor shows the design team:

➢ Kneeling in front are Dick Erdrich, Joe Dearing, Neil Macrorie, and Stan Dorr.
➢ Standing at the left are Bob Litz, John Bergman, and Jim Frazier.
➢ Standing at the right are Paul Rodriguez, Bill Zekoff, Marv Janisch, Jim Hadine, and Mel Janisch.

3.4 Trident Memory Processor

This picture was included in a UNISYS market report in 1986. It shows the Trident Navigation Center mock-up at the SSM facility. Three Memory Processors are shown in the background labeled 1, 2, and 3. My understanding of the system operation had one box running on-line, the second box was a hot back-up, and the third box was being used as a Random-Access Mass Memory (RAMM). I was told that because of the large memory provided by the RAMM a hard drive unit was removed eliminating some structure borne noise and maintenance issues

3.5 UYK-43 Demonstration

https://vipclubmn.org/cp32bit.html#UYK43 provides some technical information about the AN/UYK-43 computer.

This picture was taken in the summer of 1984 during the first demonstration of the AN/UYK-43 to Harry Gold of either NAVSEA or BUSHIPS, I don't know which. Shown right to left are Jack Metzger, Deputy Project Manager, Jim Bratsch, one of the project's mechanical engineers, and me.

3.6 Cost Savings

These pictures below involve the presentation of cost saving awards for the year 1983. Most long-time employees will understand why this came about but a little explanation might be in order for the uninitiated.

I believe that most departments within UNIVAC had some type of formal cost savings program. It could be compared to changing one of the PROCESSES that current day management is so in love with, only you were paid for it (Maybe that's the secret for updating processes; offer enough prize money and they might even become usable). The award amounts were modest but included a yearly banquet at the Officers Club in Ft. Snelling. I was aware of the program within my department, engineering, but never paid much heed as to put in a cost saving on my design would be to admit I'd screwed it up to begin with. Most of the cost savings were generated by the Engineering Support Groups such as drafting. They had quotas and were expected to generate these cost savings annually. I had the feeling that a lot of these changes were initiated in one year then taken out a few years down the road. Nonetheless I found myself deep into the program as the result of working on the UYK-43 Project.

Picture 16A (right) shows Clyde Allen, Vice-President of Engineering, presenting me with two savings bonds for my cost saving submission. The first bond was for $50.00 (Company cost $37.50) for the "Cost savings of the quarter" and the second was $100.00 (Company cost $75.00) for "Cost savings of the year".

Picture 16B (right) is Clyde presenting me with a table-top stereo as a reward for cost savings of the year. The stereo lasted about 2 years before going belly up, but I hung on to the savings bonds until 2006 and got about $260.00 when I cashed them.

The reason I even applied for the cost saving was due to Jim Andrews who was one of the support software programmers writing stuff mainly for the 1100 mainframe using FORTRAN. His group routinely submitted cost saving ideas, so I was dealing with an expert.

We had finished up the Memory Processor (MP) project in early 1983 and I assumed that I would enjoy a little "bathtub" period following a year and a half of 9-hour days, six-day weeks. You know about bathtub periods, run the tub full, immerse yourself up to the nostrils, and stay in there as long as the water's hot and hunger doesn't become a problem. Normally, bathtub periods were a natural part of projects because it was rare for new work to be sitting on your doorstep waiting for the current project to be completed. I had been without a bathtub rest for some time because the ATD, ETV-1, ETV-2, and MP projects had pretty much followed one other. I was not really happy when I was told I would be joining the UYK-43 project currently in initial checkout. I wasn't singled out though. Mel Wagner and Leo Slecta were also being brought in to help. The Central Processor (CP) was being checked out in a fixture called the cheeseboard which was nothing more than a processor chassis back panel with pins available for plugging in modules on both sides. Mel and Leo were to work with Dave Kaminski and Gene Hervig, the CP designers, in finishing CP checkout. I was to finish assembling the fan-out fixture and integrate the CP, Memory, I/O, and the Maintenance Panel. Oh, yeah, on the way I was to get the cache memory card running. Priyon Guneratne (I know I killed his name) had designed the cache memory module and left the company before it was built. With my previous cache memory experience, I didn't see anything too tough about this as the 43 cache was much simpler than that of the MP.

That fan-out crew were mostly young guys that either came from the Plant 1 test floor or were working in engineering as technicians. Some of the names were Tom Koetter, Greg Miller, Larry Stafsholt, Mark Neutz, Doug Hanson, Dave Wagner, Don Overdier, and probably others.

The 43 projects had run into rough times during initial checkout. I believe that Finley McLeod had been the original Project Manager but due to schedule slips he had been replaced by Bob Jablonski.

Bob had bounced around for a while and had originally come from UNIVAC commercial. I don't know whether taking over the 43 project was a promotion or a demotion. I had a standing meeting with Bob at 3:00 every afternoon. He was pushing me hard for integration success and I could only work as well as the chassis I received. We yelled and screamed at each other and went away mad many times, but he probably accomplished his mission, getting the checkout accomplished, even though he never picked up a scope probe.

The source of the checkout problems was the Address Control card in the CP. A major concern was the requirement to operate with both semiconductor and core memory modules. Changing from one type to another created timing problems and the requirement for deterministic timing, regardless of memory type, was driving Dave and Gene nuts. I had faced the same problem in the MP architecture but was able to convince the Navy to eliminate the need for core memories in favor of DRAMS as core was on its way out and virtually all system operation, even with core memories, performed an initial load before operation. The 43 project was not successful in getting the core memory requirement removed and it was a major headache during checkout. When a fix was installed on the individual modules it was done under an Experimental Rework philosophy. If it worked it would later be documented as an Engineering Information Release (EIR). The problem was that a huge number of changes were being made, and later changes were removing or modifying earlier changes. If any mistake was made in the jumper wires used to make the cuts and jumpers it could get lost in the mass of wiring building up on the boards. Before I arrived on the project the Address control board printed wiring had gone back through layout after over 1000 jumper wires had been added. When I arrived, the count was already back to almost 900 on the new board and eventually ended up close to 1100. Troubleshooting these boards was very difficult because of extra wires. If a rework jumper was installed incorrectly it could be wrong on one or both ends. Many times, there was an existing wire on the Integrated Circuit (IC) pins and there was no way to tell whether that wire belonged there or not. An extra wire doesn't manifest itself as something not happening like a missing wire would, but as something happening that doesn't make sense.

And then, an unintended stroke of brilliance out of sheer frustration. What we really needed was a computerized data base that would list all the IC pins on the module and note the number of rework wires on each pin. I've had many good ideas over the years and, if I couldn't do it myself, let them go. In this case though, the UYK-43 deputy project manager, Jack Metzger, was a pretty good guy and would listen to my argument. I laid out what I wanted, and he found the money to fund it. The next step was to get a hold of Jim Andrews, whom I mentioned at the start of this, and see what could be done. He understood the problem and dug into it. Within a couple of weeks, he had a FORTRAN Program, called "Rework" ready for use and I recruited Tom Koetter from the fan-out crew to input all the EIRs for the Steering module.

The output was the resulting interconnection nets after all the EIRs had been applied. This module did a lot of sequencing and timing and had a modest number of jumper wires, ~350. Tom was an old hand at working with computer applications and had the EIRs into the data base in a few days. Jim made the first run of the now termed "Rework" Program and we had our first rework inspection list.

We had several steering cards available to us, all in various stages of inoperability, so we picked one that we had never had any luck with and sent it off to prototype manufacturing for inspection. They had it for about a week and were constantly calling the fan-out crew to help them unhook and terminate the wires. You have to understand that these wires were run between ICs (Integrated Circuits) and most could not be traced from one end to the other. If a pin was supposed to be empty and a wire was found soldered to it the wire was removed and buried in the bundle. When the inspection was done we plugged the module into a chassis, and it worked!

From that day on things started going right. Tom proceeded to input EIRs into the data base for all the other modules. Every module went through rework inspection, and we were able to establish a solid baseline at the fan-out. Gene Hervig had gone on sick leave during this time and when he returned the CP checkout progressed rapidly and I believe we made the schedule milestones we were shooting for.

Sometime after all of this excitement Jim Andrews looked me up to consider submitting the Rework Program as a cost savings. His rationale was that without it, the 43 program would still be in checkout and would not have made any schedule. I agreed to support him with the understanding that we would split the cost saving three ways but because it was my idea I wanted 34% and he and Tom could each have 33%. He agreed to do all the paper work and try and establish the cost saving value. I think the first cut we had the value as something over $16,000,000. He submitted it and it was rejected. He mentioned at the time that upper management did not like the number because it might imply that they were not doing their jobs. He resubmitted the proposal and eventually settled on a value of about $2,200,000 of which $750,000 was mine. At the time, and probably to this day, this was the highest value cost saving recorded.

I have been told by guys that worked on the 43 programs for many years that no computers were delivered with core memory modules. Go figure!

EPILOGUE

Dr. Erdrich

In the 80s while developing the Memory Processor (MP), Dick made many, many presentations about computer architectures, especially how cache memory worked and how 24-bit addressability and the MP register/interrupt architecture would facilitate context switching of the ADA language. One day he came to me, Lowell with a poser. "I received a letter from a professor out east addressed to Dr. Erdrich." The letter was asking him to make a technical review of a book about computer architecture. Dick asked how he should reply. My suggestion was to go ahead and do the review, collect any 'cash' being offered, and just sign any correspondence, 'Mr. Richard Erdrich.' He did not need to comment about not having a Doctoral degree – even though his detail computer knowledge was at that level. Mr. Erdrich is among very few at UNIVAC/Unisys/Lockheed Martin who could talk about top-down architecture while designing and making machines from the component interconnect level up! *LABenson*

Salt Lake City

In the early 90s, diminished defense budgets meant less work for Unisys defense industry engineers, thus there were layoffs every six months. A small group of engineers including Dick were sent to Salt Lake City to aid in the development of wide band systems. He and others were there from April 1993 until March 1997.

The Rest of the Story!

From 1998 until his retirement in 2006, Dick worked on a plethora of designs that included updates to the B-2 ACU computers and updates to the P-3c's CP-2044. His final project was the Quad Processor for the Joint Strike Fighter (F-35), https://vipclubmn.org/computersAF.html#JSF.

After 47 years, 4 months, and 13 days I didn't feel as though I needed to hang around just to watch another processor run. Its' been a heck of a journey!   Dick

{Editor's note: The projects mentioned as the *Rest of the Story* are detailed in the June 2025 Our Stories: https://vipclubmn.org/Articles/Erdrich4th.pdf.}