ERA to UNISYS TECHNOLOGIES

Computer Technologies Spanning Five Decades Are Exhibited on the History Wall
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ERA to UNISYS TECHNOLOGIES

INTRODUCTION

Five decades of new computer systems' technologies started in 1946 with Engineering Research Associates (ERA); the beginning of our Information Technology (IT) Legacy. In 2005, the UNISYS and Lockheed Martin retirees VIP CLUB started their IT Legacy Committee with the expressed purpose of preserving this fascinating history.

Sperry-UNIVAC in Roseville had an earlier sense of history in the 80s, thus began to illustrate computer technologies with a series of wall mounted shadow box displays. Harry Smuda [Management] and Dick Petschauer [Engineering] created these shadowboxes.

After the Burroughs buyout of Sperry in 1986; the resulting UNISYS Company kept the displays - adding to them as new commercial computer systems were developed in the 90s.

This paper illustrates and documents the computer sequence of the Unisys 'history' shadowboxes for research by computer technology historians. Mike Svendsen transcribed the shadow box 'plaque' text as written in the various sections hereunder.

COMPUTER SYSTEMS

1955 – 1103 System

In 1955 the 1103 System[1] had 10,000 gates using vacuum tubes.

The basic logic element had 25 gates with a speed of 2 microseconds per gate. {Editor's note: the tube chassis shown below was the logic element.}


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[1] The 1103 was the commercial version of the then classified ATLAS II.

Wired connectors [right] were used with soldered point to point wiring with 44 connections per square inch. The storage was 4,096 bits of core with a cycle time of 14 microseconds and a capacity of 16,000 characters. The cost for 4K was $6,144. {Editor's note: Tree diagram below from Ron Q. Smith shows the UNIVAC 1103 as following the original ERA 1101 computer, a commercial version of the ATLAS I.

Family Tree of Remington Rand/Sperry Rand Computers 1950-1963
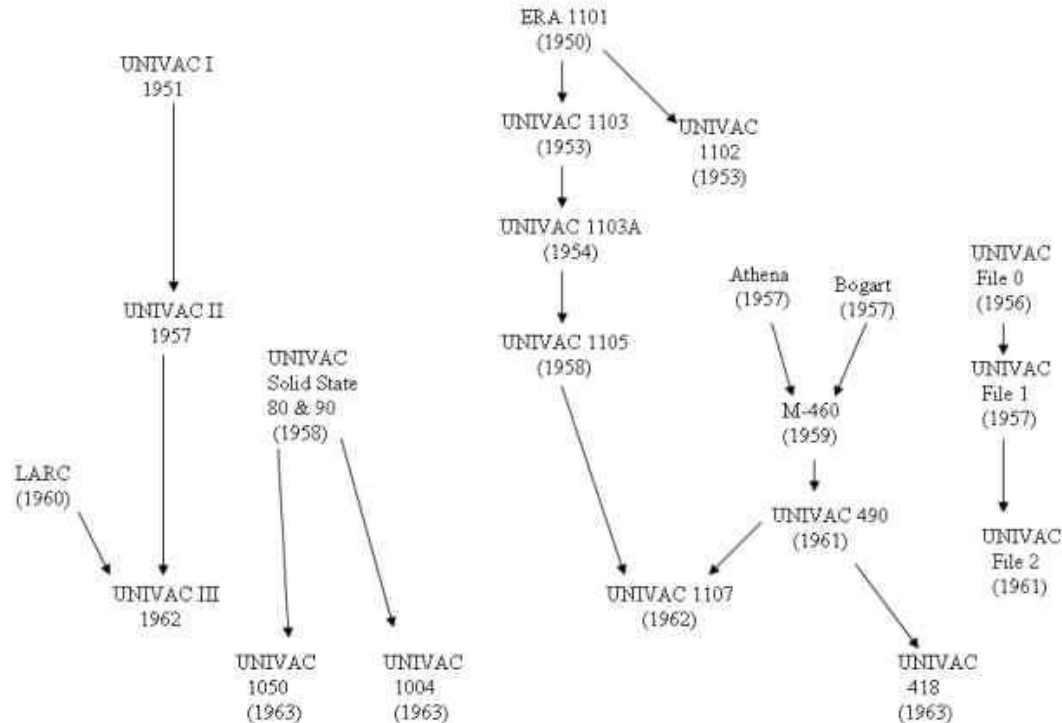
The UNIVAC computers and the LARC shown at the left of this tree were developed and produced in Blue Bell, PA – continuation of computers developed by Eckert Mauchly Computer Corporation. In the right center; the St. Paul developed Athena was the NASA missile launch computer and the Bogart was a classified machine. The M-460 was the commercial version of the Navy Tactical Data Systems' 1958 AN/USQ-17 computer – prototyping the commercial 490 series of 30 bit computers.}

1961 – 1107 System

In 1961 the 1107 System had 20,000 gates using transistors. The basic logic element had 20 gates with a speed of 80 nanoseconds per gate.

The connectors and back panels were wire wrapped and used PC cards with 9 edge connectors resulted in 16 connections per square inch. The storage was 4,096 bits of core with a cycle time of 2 microseconds and a capacity of 393,210 characters.
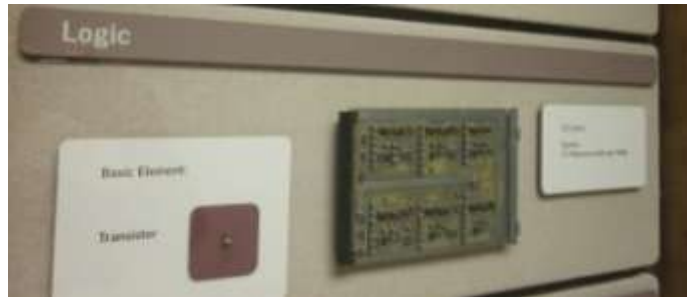
1965 – 1108 System

In 1965 the 1108 System had 30,000 gates using transistors. The basic logic element had 50 gates with a speed of 15 nanoseconds per gate.

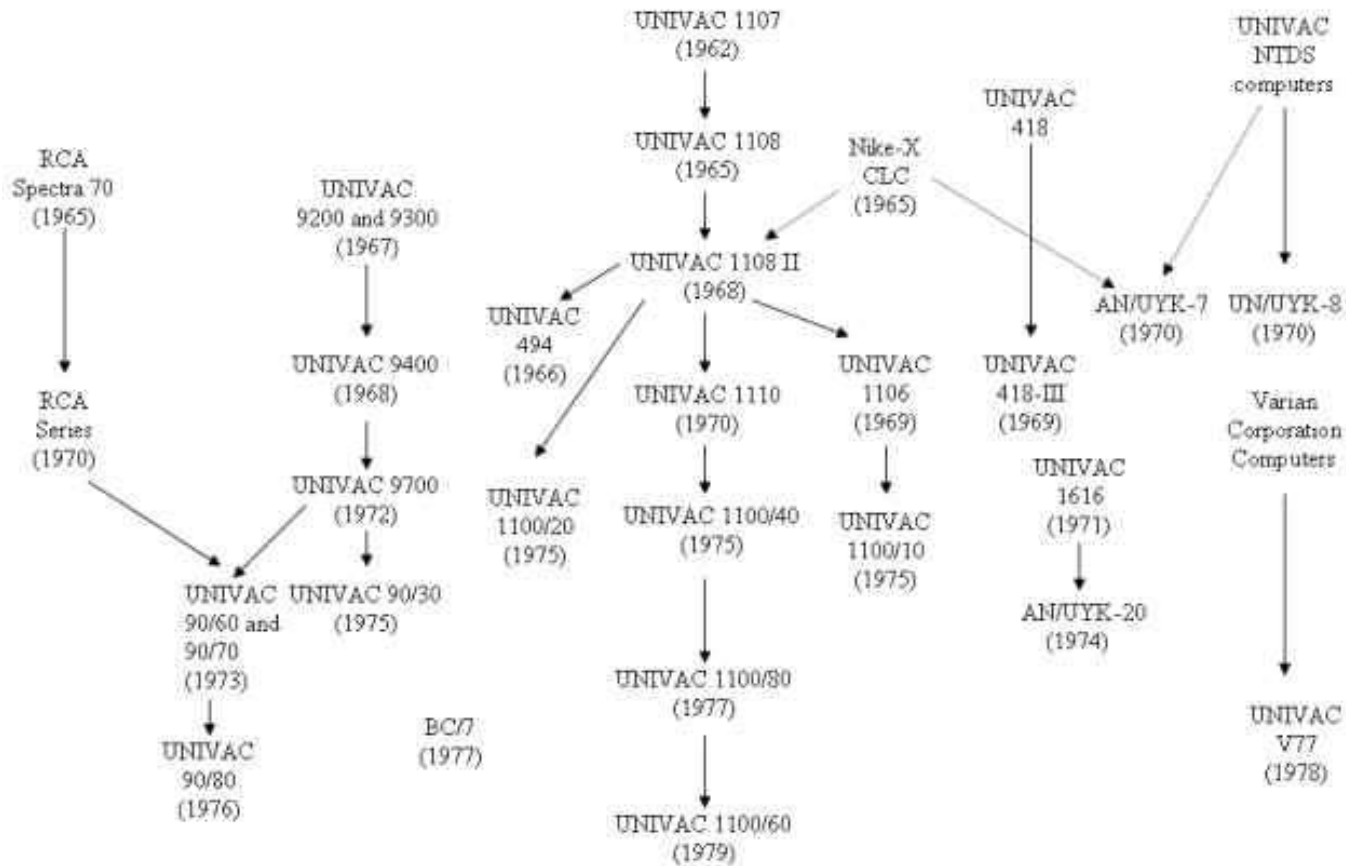The wire wrapped back panel and cards resulted in 44 connections per square inch.
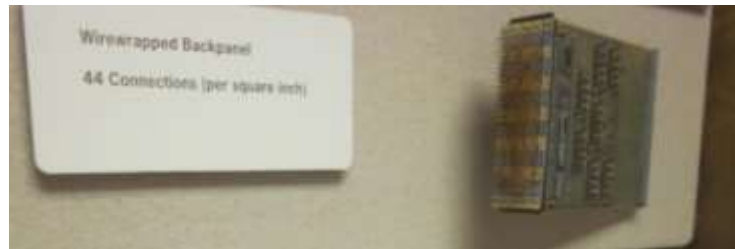
The storage was 4,096 of core with a cycle time of 0.75 microseconds and a capacity of 1,000,000 characters.

{Note: Unisys Fellow Ron Q. Smith's 2nd tree shows the 1107 of the previous tree on page 3 leading into the 1108 and subsequent computers developed by the Roseville, MN engineers. The 1965 Nike-X CLC provided the multi-processor techniques for the 1108 II.}

Family Tree of Sperry Rand Computers
1962-1980

1972 – 1110 System

In 1972 the 1110 System had 170,000 gates using integrated circuits with 200 gates (SSI) and a speed of 12 nanoseconds per gate.

The wire wrapped connectors with SSI soldered to card resulted in 44 connections per square inch. The storage was plated wire with a cycle time of 0.28 microseconds and 1,000,000 characters. The cost for 4K at the system level was $163 and only represented 6 % of the memory rack.
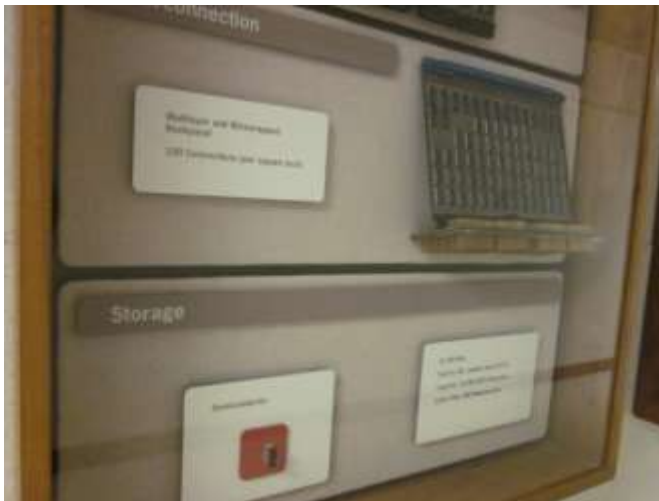
1978 – 1100/80 System

In 1978 the 1100/80 System had 180,000 gates using integrated circuits with 900 gates (MSI) and a speed of 6 nanoseconds per gate. There were 64 MSI's on a card.

The multi-layered wire wrapped back panel resulted in 100 connections per square inch. The storage uses 16K bit semiconductor memory devices and the system level cost was $5 for 4K. The cycle time was 650 nanoseconds with a capacity of 32,000,000 characters.
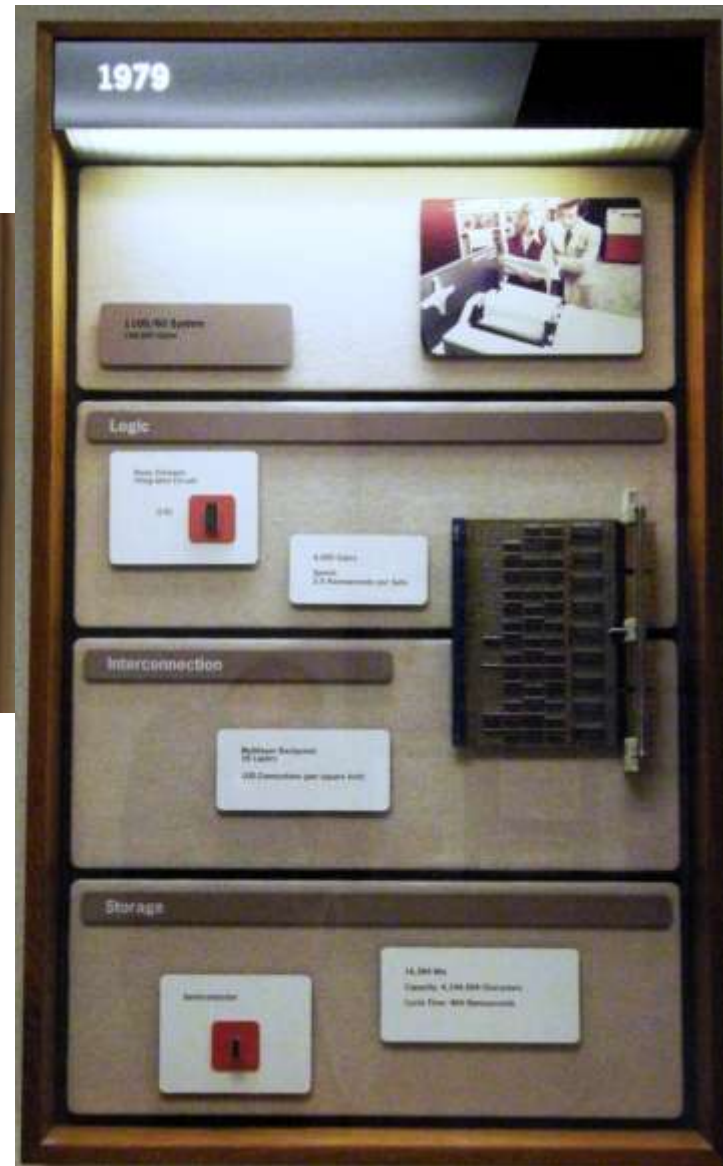
1979 – 1100/60 System

In 1979 the 1100/60 System had 148,000 gates using integrated circuits with 4,000 gates (LSI) and a speed of 2.5 nanoseconds per gate. The multi-layered back panel resulted in 100 connections per square inch.

The storage uses 16K bit semiconductor memory devices with a cycle time of 464 nanoseconds and capacity of 4,194,304 characters.
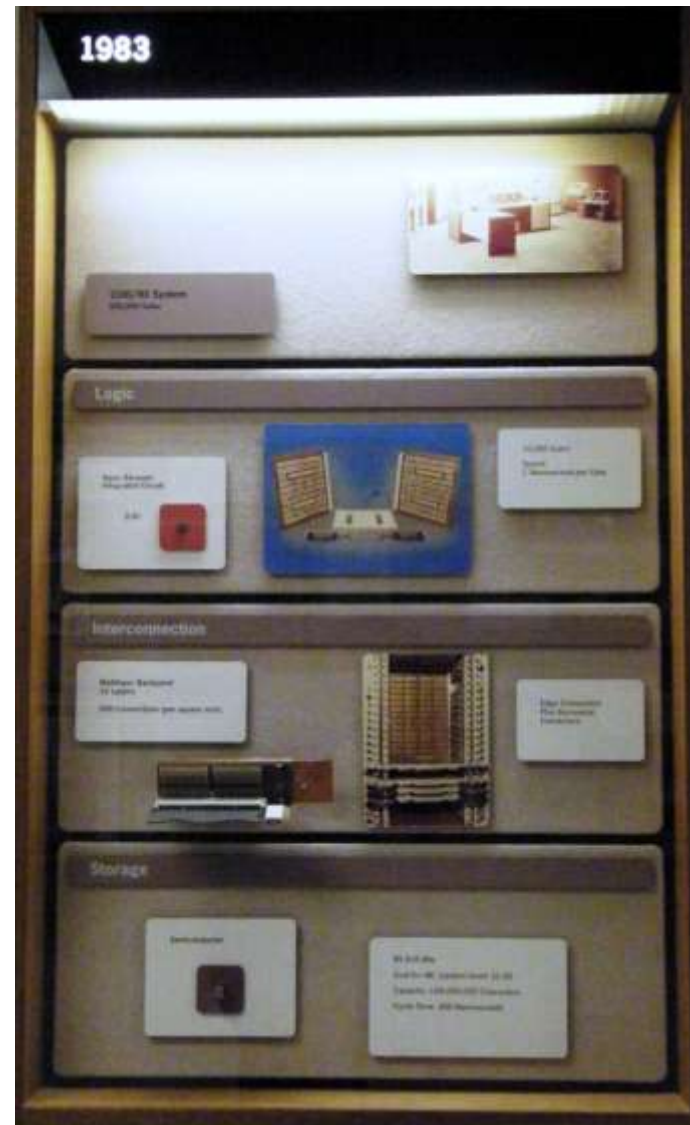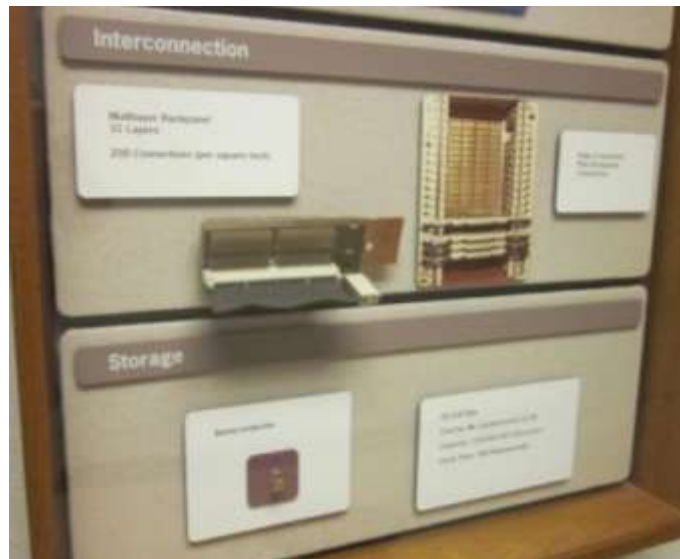
1983 – 1100/90 System

In 1983 the 1100/90 System had 500,000 gates using integrated circuits with 10,000 gates (LSI) and a speed of 1 nanosecond per gate.
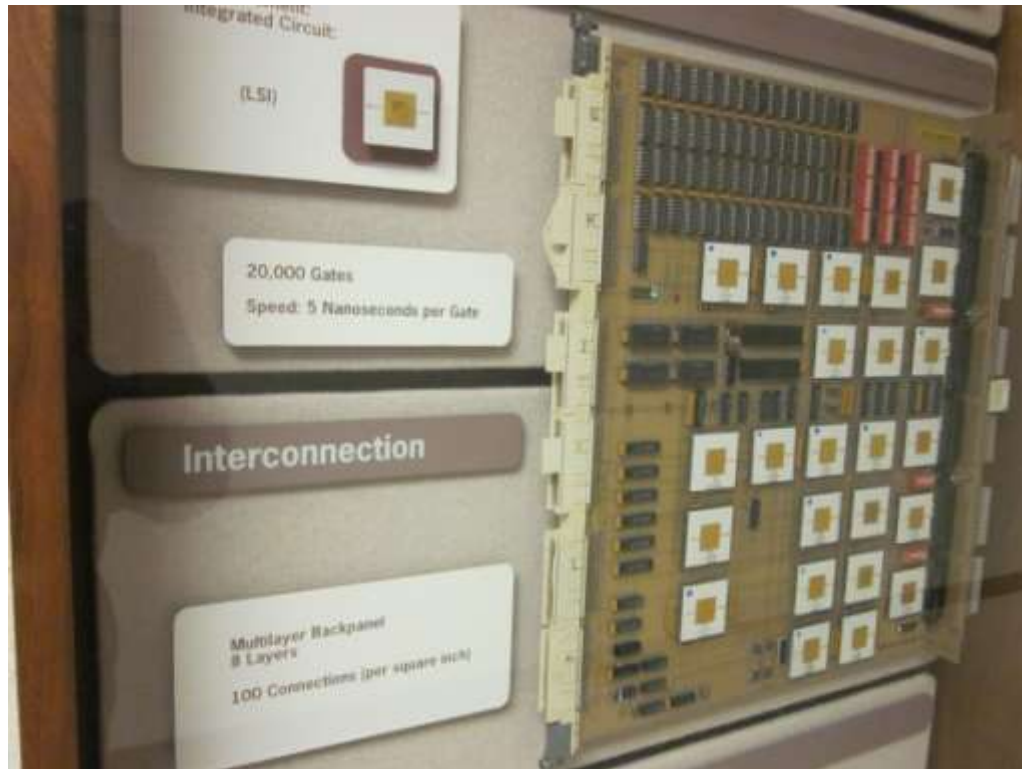

The multilayered back panel had 31 layers with edge and back panel wire wrapped connectors resulting in 200 connections per square inch. The storage uses 64K semiconductor memory devices with a cycle time of 360 nanoseconds and a capacity of 128,000,000 characters. The cost for 4K at system level was $2.50.

1985 – System 11

In 1985 the System 11 had 170,000 gates using integrated circuits with 20,000 gates (LSI) and a speed of 5 nanoseconds per gate.
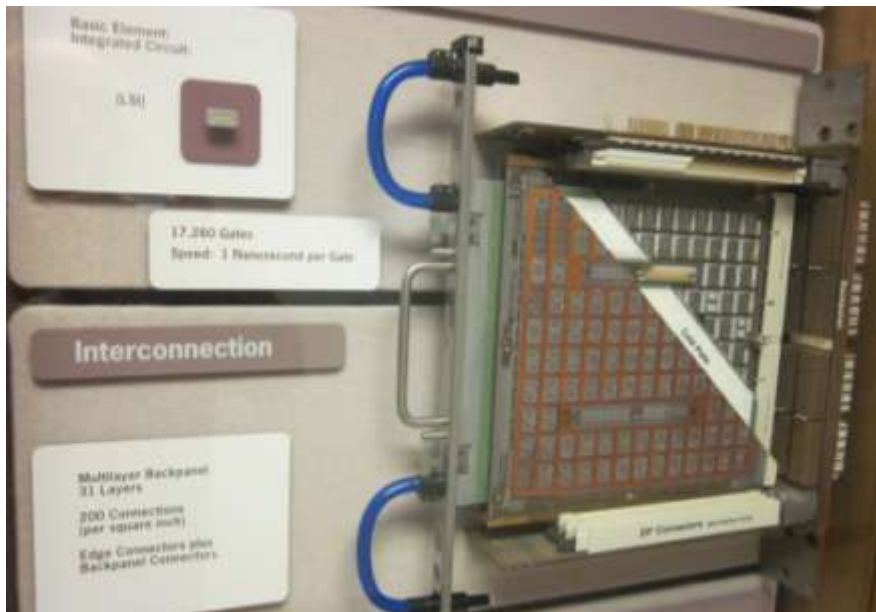

A drawer has 24 LSI and a back panel with 8 layers resulting in 100 connections per square inch. The storage uses 64K semiconductor memory devices with a cycle time of 300 nanoseconds and a capacity of 4,194,304 characters.

1985 – Integrated Scientific Processor

In 1985 the Integrated Scientific Processor had 1,726,000 gates using integrated circuits with 17,260 gates (LSI) and a speed of 1 nanosecond per gate.

The multilayered back panel has 31 layers with zero insertion force (ZIF) edge and back panel connectors resulting in 200 connections per square inch. The LSI are mounted on both sides of a liquid cold plate.

The storage uses 64K semiconductor memory devices with 8 to a card with a cycle time of 90 nanoseconds and a capacity of 128,000,000. The cost for 4K is $8.25 at the system level.
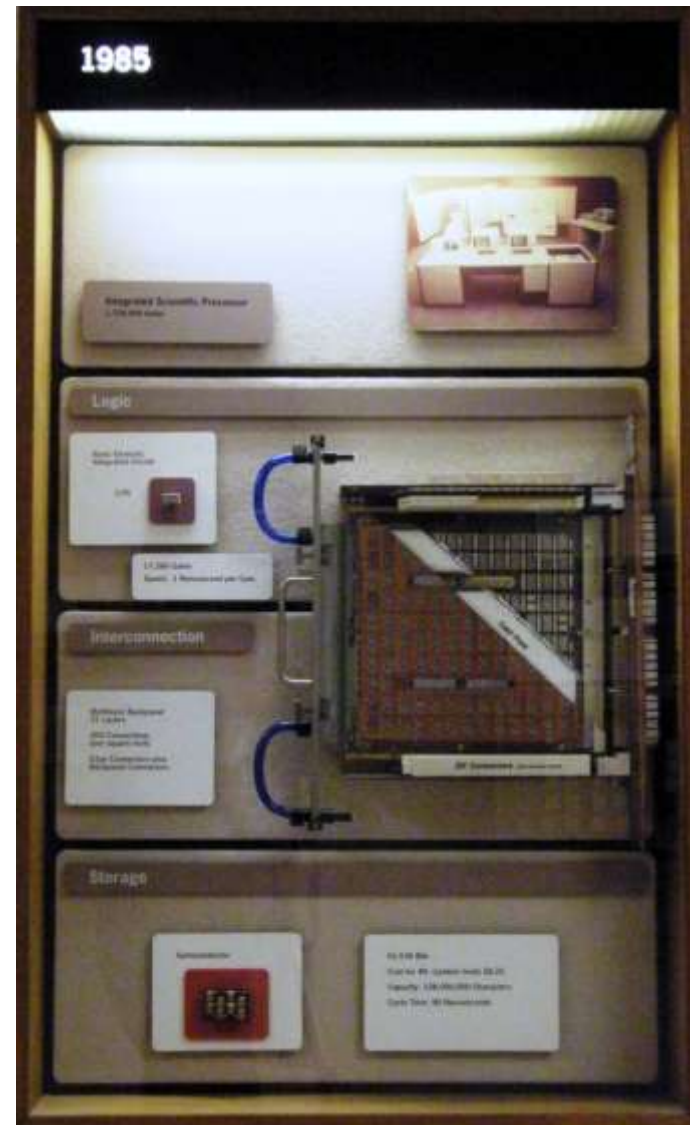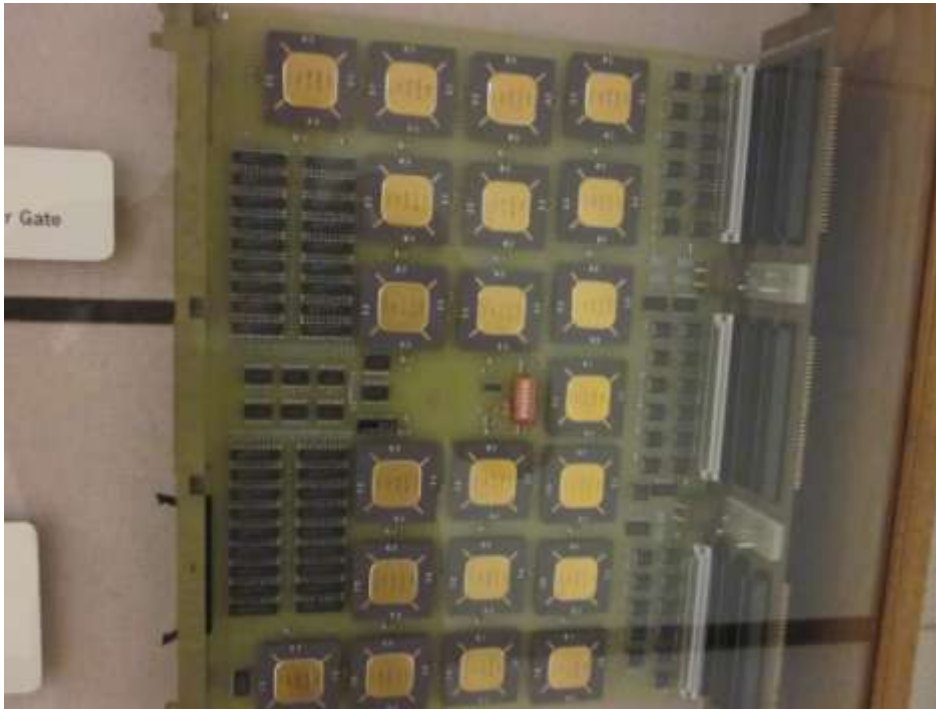
1987 – 2200/200 System

In 1987 the 2200/200 System had 200,000 gates using integrated circuits with 100,000 gates (CMOS VLSI) and a speed of 6 nanoseconds per gate.

The multilayered back panel had 8 layers and resulted in 100 connections per square inch. The storage uses 256K semiconductor memory devices with a cycle time of 432 nanoseconds and a capacity of 50,331,648 characters.

1989 – 2200/400 System

In 1989 the 2200/400 System had 250,000 gates using integrated circuits with 125,000 gates (CMOS VLSI) and a speed of 5 nanoseconds per gate. There were 25 VLSI per chassis.
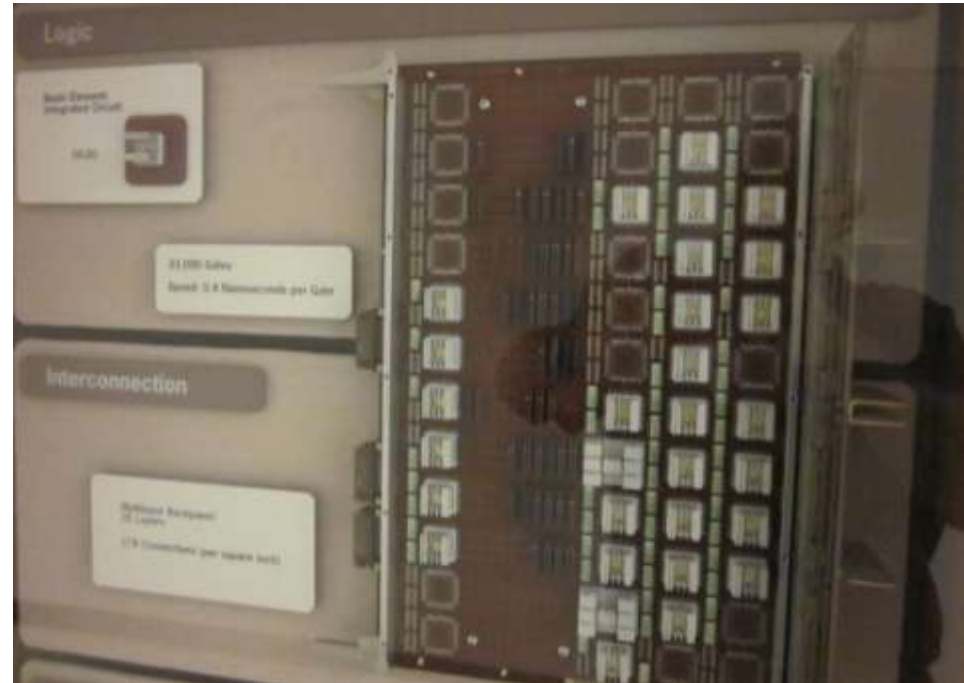

The multilayer back panel resulted in 100 connections per square inch. The storage uses semiconductor memory devices with 1,048,576 bits with a cycle time of 112.5 nanoseconds and a capacity of 67,108,864 characters.

1989 – 2200/600 System

In 1989 the 2200/600 System had 600,000 gates using integrated circuits with 33,000 gates (VLSI) and a speed of .4 nanoseconds per gate.

The multilayered back panel has 26 layers and a complete chassis had 28 VLSI and 278 connections per square inch.

The storage uses semiconductor memory devices with 1,048,576 bits with a cycle time of 82.5 nanoseconds and a capacity of 67,108,864 characters.

1992 – 2200/900 System

In 1992 the 2200/900 System used Motorola's MCA9K Bipolar ECL integrated circuits with 9000 gates and a speed of 100 picoseconds per gate.

The semiconductor memory used many different technologies striving for optimum speed. There were 3 levels of storage:

- First Level Cache used 4K Bit Ram,
- Second Level Cache used 16K and 64K Bit Rams, and
- Main Storage Unit with 1024 Megabytes used 64K Bit BICMOS SRAM (12 nanoseconds), 4K Bit ECL SRAM (3 nanoseconds) and 4 Megabit CMOS DRAM (70 nanoseconds).
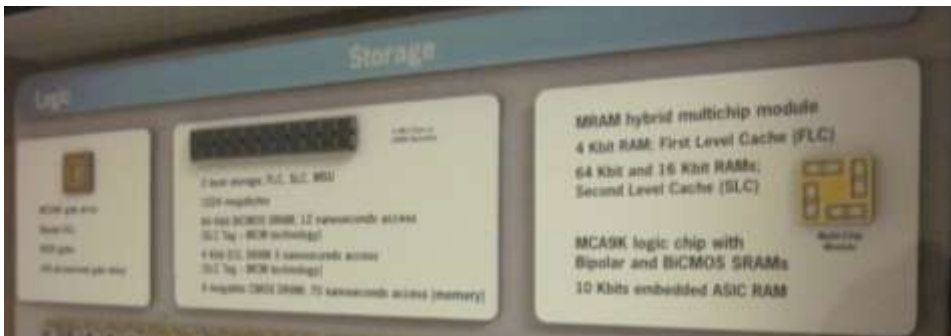
The following pictures show an actual DiMM assembly with eleven 4 Megabit chips, a MRAM Hybrid Multichip Module, a MCA9K Logic chip with Bipolar and BICMOS SRAMS (10K Bits) embedded within the ASIC. There is also a completely populated chassis.

The very dense printed circuit boards had 50 layers, were water cooled and utilized high speed dielectric materials with low temperature solders resulting in 53 connections per square inch.
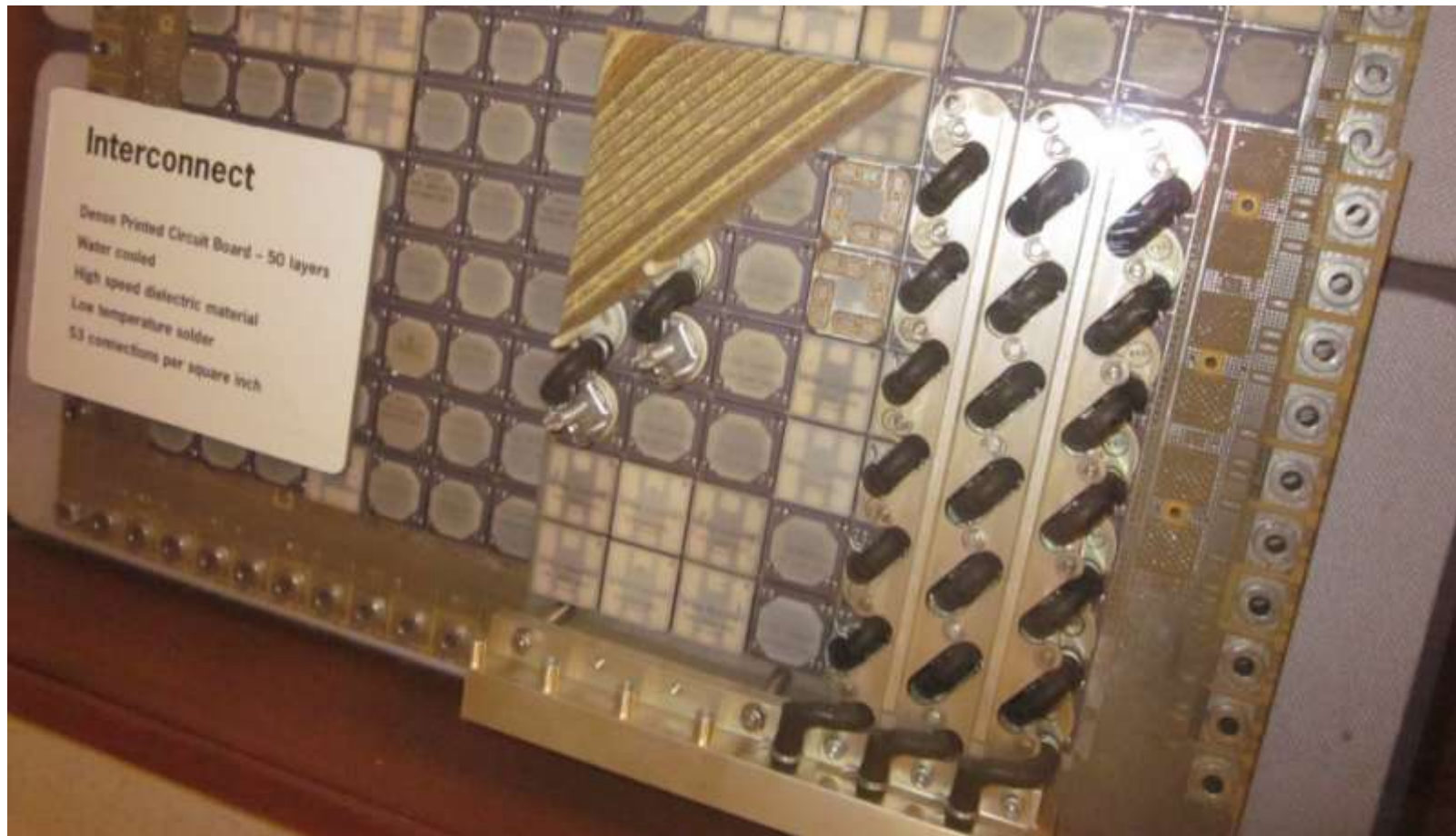
1993 – 2200/500 System

In 1993 the System 2200/500 used Motorola's H4C CMOS VLSI (318,000 gates) built with .8 micron technology and a 500 picoseconds gate delays.

The 26 layer IP PC Board had devices on both sides with cooling fins.

The back panel contained ASICS with double sided mounting on the Main Storage board resulting in 26 connections per square inch.

The semiconductor memory contained 1024 Megabytes and used 16K Bits of Embedded ASIC RAM, 256K Bits of CMOS SRAM (20 nanoseconds) and 16 Megabit DRAM (60 nanoseconds.)

Interconnect

Active backpanel (contains ASICs)
26-layer IP printed circuit board
Double-sided mounting on MSU board
26 connections per square inch

Storage

1024 megabytes
16 Kbits embedded ASIC SRAM
256 Kbits CMOS SRAM;
20 nanoseconds access
16 megabit DRAM;
60 nanoseconds access
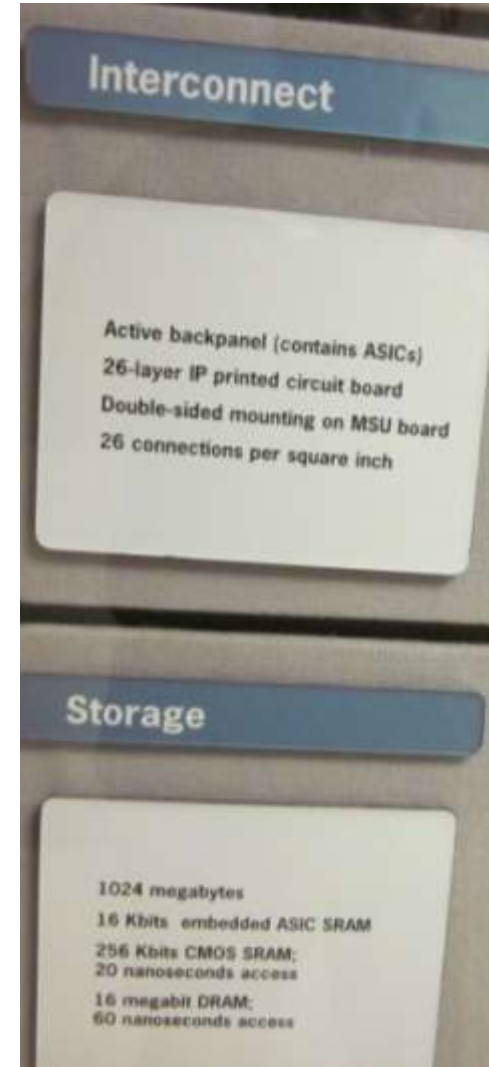
1995 – eXtended Processing Complex

In 1995 the eXtended PROCESSING COMPLEX - XPC demonstrated many computer architecture advancements along with the hardware innovations. There were more than 70 patents reflected in the XPC. Parallel processing via multiple processors, post store system data caching, multi-host record locking and quad redundant clock for fail safe distribution were some of the innovations.
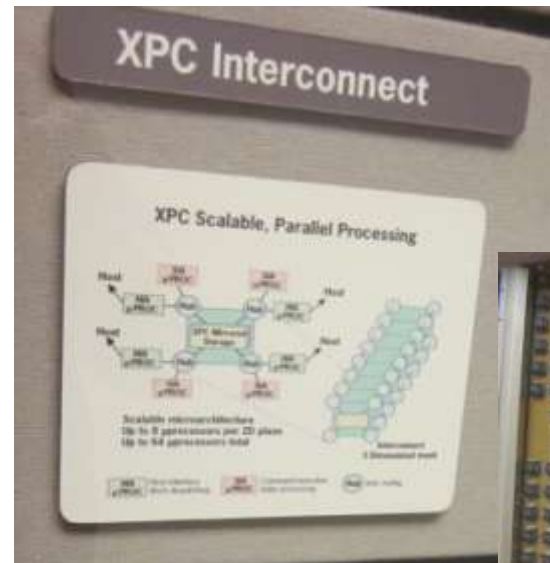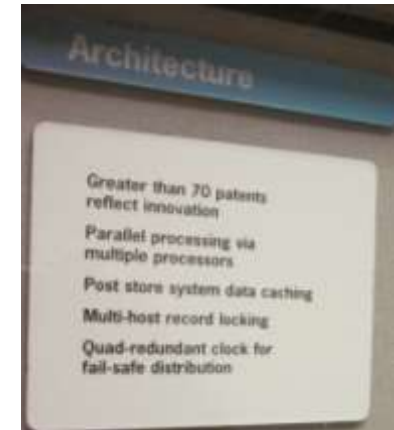
The interconnection was with fiber optics. The main storage was with 16 Megabit Drams with 60 nanosecond access.
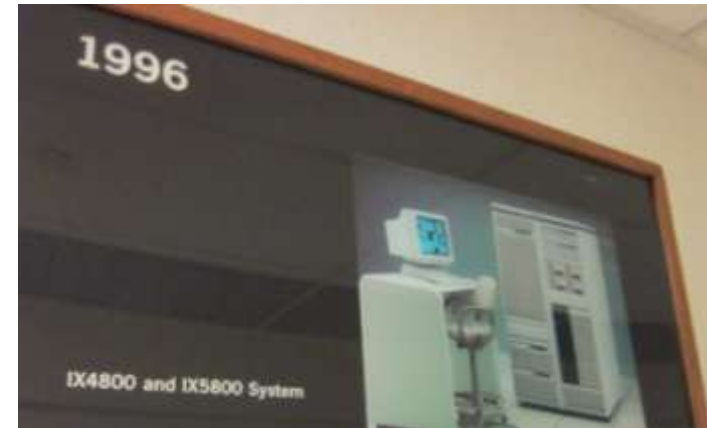
There were 80,000 gates in the system using UNIVAC's 1.0 micron CMOS gate arrays each with 448 gates.
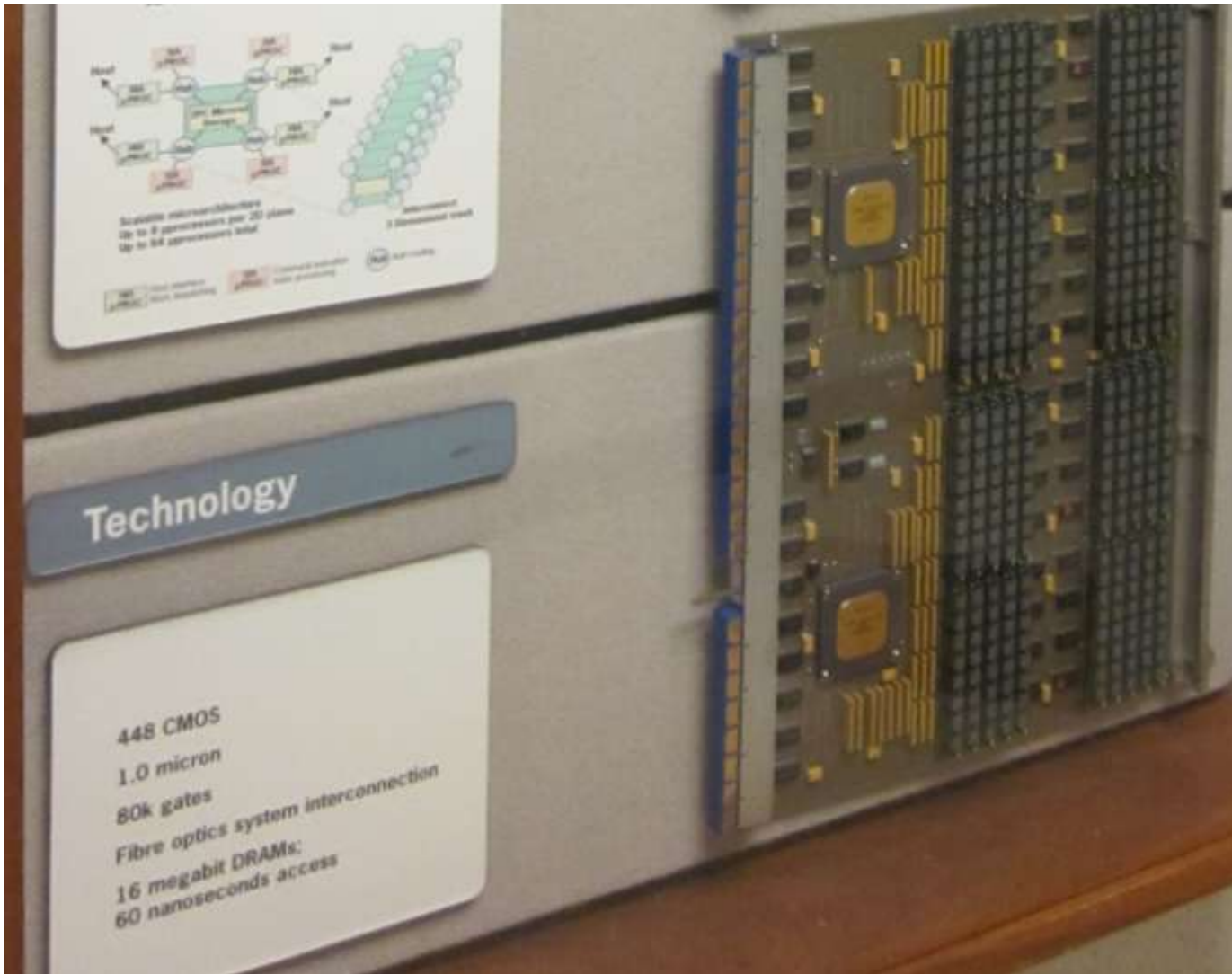
1996 – IX4800 and IX5800 System

In 1996 the IX4800 and the IX5800 were built using IBM's C5L .5 micron CMOS with 1,557,000 gates per chip. There was 2.155 Mega Bits embedded ASIC RAM per chip.

The PC Boards had 22 layers and used solder column ASIC attachment resulting in 32 connections per square inch.

The storage had 3 levels with 4.5 Gigabytes of Main Memory. It also used 1 Megabit CMOS Pipelined SRAM (4 nanoseconds) and 16 and 64 Megabit Drams (60 nanosecond.) .

ACKNOWLEDGEMENTS

During 60$^+$ years; computer technologies have evolved from vacuum tube logic through transistors to integrated circuits with just a few single gates to over a half million equivalent gates in a device. We, the retirees of the ERA to UNISYS corporate transitions, have been involved in all aspects of the technologies growth. It was very exciting and rewarding to be involved and I hope this paper has given the readers an overview of some of the ERA/Univac/Sperry/UNISYS technologies in computer history.

Bernard N. "Mike" Svendsen.

Author

I graduated in 1959 from the University of Minnesota with a Bachelor of Science degree in Electrical Engineering. I had asked my uncle [Commander Edward C. Svendsen] if he had any thoughts about the electronics industry and where I might go to work. His comment was brief: "well, UNIVAC is doing some interesting things with computers". UNIVAC was close to home so I joined in Aug '59. The semiconductor industry was in its infancy then and the majority of my 25 years at Univac were involved in semiconductor specification, design, evaluation, testing, quality, failures, cost, availability and manufacturing at our suppliers and at our in-house facility. You might say we matured together.

I worked at all of the plants in the Twin Cities and in many disciplines: Electrical Engineering, Reliability, Test, Procurement, Quality, Production, Quality Assurance, Operations Management, Bipolar Operations and the Semiconductor Control Facility. I was a member on Sperry's Corporate Councils on Semiconductors, Standardization and Procurement.

Editor

Lowell A. Benson, BEE 1966 - U of MN. Mr. Benson was a UNIVAC 1960 to UNISYS 1994 employee. He has served on the VIP Club Board for nine years and has been co-chair of the IT Legacy Committee since its inception in 2005.

The file name of this paper is ERA2unisys, the micro-technology shadowboxes of the history wall are documented in file univac2unisys. Snapshots in this paper were taken by Mike and Lowell.