INTEGRATED CIRCUIT STANDARDIZATION WITHIN DEFENSE SYSTEMS DIVISION

by

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The potential improvements in size, power, performance, reliability, and cost available with semiconductor integrated circuits have received a great deal attention throughout the electronic industry. From the start, digital switching applications have received the major benefit from this new technology, due to process requirements well within the state-of-the-art and also due to the large number of repetitive functions inherent in most digital machines. Continuing its leadership in the application of new techniques, the UNIVAC Defense Operations in St. Paul was one of the first systems manufacturers in the United States to actively investigate and use integrated circuits. The purpose of this paper is to summarize the growth of this field within Defense and to discuss in detail progress during the last 12 months toward a "Standard" integrated circuit family fulfilling the earlier mentioned promises.

The first significant step taken by Defense was a development contract with Sperry Semiconductor as part of the ADD program. This effort during 1960-61 proved to be premature but did form a basis for future planning and funding. An engineering group was set up to centralize our activities during 1962 but it was not until early 1963 that major emphasis was placed on the entire microelectronics field. At that time the decision was made to become a major factor in the Aerospace business and an entire department was organized to handle this work. The 1824 computer used on such programs as MMRBM, BGRV, MBRV, and SABRE required the design of the first integrated circuit family used in UNIVAC. The circuits were packaged in a 10 pin $\frac{1}{4}$ x $\frac{1}{4}$ inch flat pak which was the industry standard at that time. An extensive vendor evaluation was conducted before Westinghouse and Signetics were selected as the primary sources. Although active work on the circuits started during the Spring of 1963, they are still in volume use today with only minor modifications. The 16 circuits comprising the family consist of six logic, eight memory, and two I/O circuits. The characteristics of the six logic circuits involved are shown in Figure 1. This family was designed with minimum part count, minimum power, maximum noise margin, and maximum reliability as primary considerations. This resulted in a compromise on type count, speed, and cost although the early date of this development must be remembered in comparison to recent performance and process improvements.

	Characteristic	"1824"
1.	Package	10 Lead Flat Pak
2.	Fanout	5
3.	Collector Logic Capability	No
4.	Operating Temperature	0° to +125°C
5.	Power Per Inverter (Avg.)	5 MW
6.	Noise Margin (Minimum)	.5V
7.	Supply Voltages	4V
8.	Propagation Speed (Typ.)	50 NS

FIGURE 1

During late 1962 a contract was negotiated with the Department of Navy for the large scale high speed CP-667 system. Due to speed and availability considerations, the decision was made to develop a hybrid chip circuit rather than a monolithic fully integrated device. At that time, Motorola was the leading proponent of hybrid devices and also the number one supplier of semiconductor devices to UNIVAC. A development program was started during the Winter of 1962-63 requiring four logic diode types, one dual transistor gate, and three memory diode types. Each of the types was packaged in a low silhouette 10 pin TO 5 package. Military certified devices were delivered during 1963 and 1964 which satisfactorily met the electrical specifications but which subsequently developed a serious failure mode during the system qualification test. A photograph of the internal construction of a typical chip circuit is

shown in Figure 2. The thermo-compression bonding technique (stitch bonding) used to attach the one mil aluminum internal wires to the active or resistive chips and to the bonding pads, was proved to be less reliable than other bonding techniques and subject to extreme process variations. Although the percentage of devices which failed in the computer was quite low (0.1% or less) the complexity of the machine and its environmental requirements required a failure rate much closer to zero.

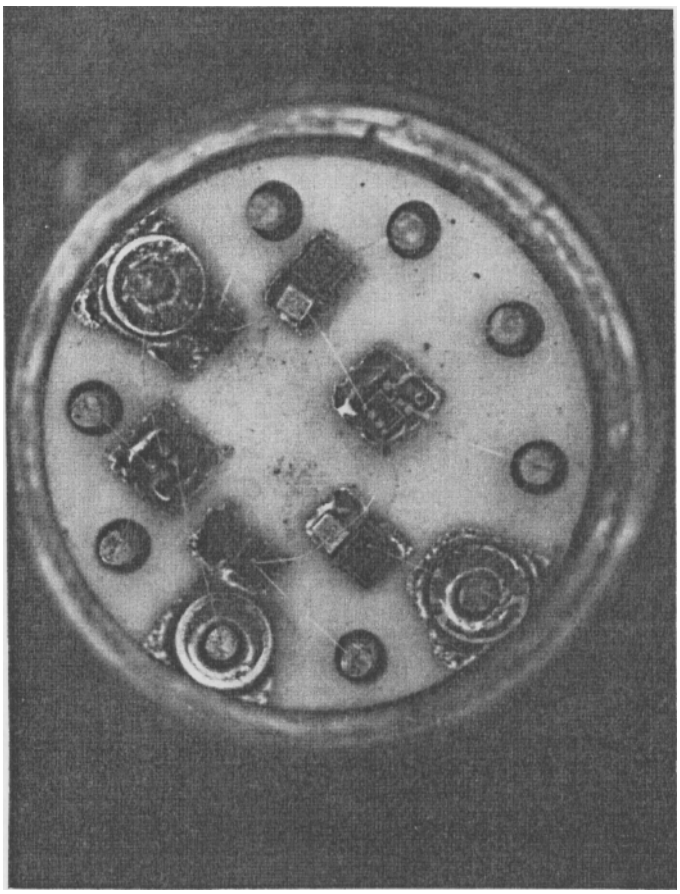


FIGURE 2

It was at this point that the reliability advantages inherent in silicon monolithic integrated circuits, and the rapidly improving performance available using this technique became attractive. A study conducted by UNIVAC had concluded in August of 1964 that the performance required for the CP-667 system was attainable with fully integrated technology and that the major failure mode of the chip circuits was significantly reduced with monolithics. Although a limited development program had been started early in 1964 to obtain monolithic circuits for this application, the effort was expanded in November of 1964 through the cooperative efforts of Reliability, Design Engineering, and Purchasing personnel. This work was partially sponsored by the Bureau of Ships with the ground rule that printed circuit cards using monolithics perform the same functions and be interchangeable with cards using hybrid circuits.

Originally it was felt that three variations of the basic circuit should be developed: a dual four input gate, a triple gate having 2, 3, and 4 inputs, respectively, and a quad, two input gate. In addition, the possibility of

CIRCUIT COUNT FOR CP-667 CENTRAL PROCESSOR

3-3 and 2-4	4-4	4-3-2	4-4 and 2-2-2-2	4-4 and 4-3-2 and 2-2-2-2
10 Pin	14 Pin	14 Pin	14 Pin	14 Pin
12K	11K	9K	7K	6K

FIGURE 3

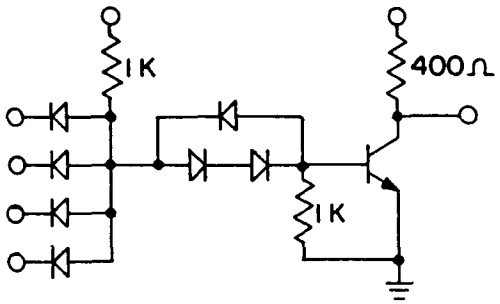
using the master slice approach was considered. This would have meant one set of masks for all three circuit types, except for the final metalization masks. Due to the potential volume predicted for 1966 and beyond, most of the vendors preferred to optimize each set of masks and each chip size for the specific circuit involved. Figure 3 shows the approximate number of circuits required in a

667 central processor for various combinations of the circuits. Since keeping the number of circuit types to a minimum was considered an important goal, the dual and quad gates were selected for development. It was felt that the triple gate could be obtained on a short turn around development at some future date if a real need was shown.

Every semiconductor vendor known to have capability in the integrated circuit field was given an opportunity to participate in the early phases of the pre-contract negotiations. Purchase part drawings had been written earlier so there were no last minute changes in scope or direction. Seven vendors indicated a desire to work with UNIVAC on the shared cost development program. The final selection of five vendors was based on past performance, long range projected pricing, vendor interest in participating, and our judgment on their capabilities. Purchase orders were placed with each of the five vendors during the first week in December of 1964. The orders defined expected delivery date, process monitoring requirements, the necessity for semimonthly status reports, milestone dates that the vendors progress would be charted against, termination provisions, and UNIVAC's qualification criteria.

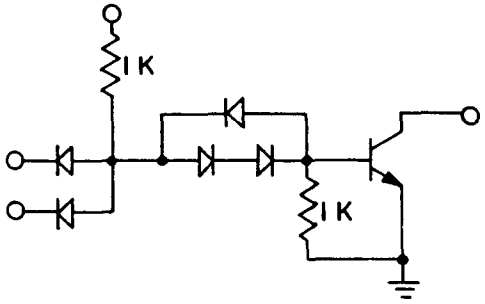
Although an equivalent circuit was shown on the purchase part drawings for guidance, the vendors were allowed to use any technique which would meet the electrical requirements. The various configurations submitted by the three vendors actually delivering parts are shown in Figure 4. The multiple emitter input transistor used by Signetics with the promise of higher speeds, unfortunately, had a reduced noise margin when compared to the normal input diodes used on the Westinghouse and Motorola chips. It subsequently became obvious that the only way for Signetics to correct this problem would be to completely redesign their masks. The early problems which Motorola encountered were apparently due to their reluctance to use the buried layer technique for reducing collector resistance and capacitance. A brief summary of our experiences with each of the five vendors is shown in Figure 5. A review of this summary indicates that Westinghouse has performed quite well, Motorola just recently demonstrated its capability to meet our requirements, Signetics delivered samples but could never meet all of the drawing requirements, and TI and Fairchild never produced electrically good units.

It is rather interesting to review photomicrographs of representative chips submitted by the two successful vendors. Figure 6 shows a Westinghouse dual gate (7901000) using a 50 x 52 mil chip with aluminum metalization and one mil ball bonded gold wire. Although this chip is very well laid out, several disadvantages exist. Two extra wires and bonds are required to get from the ground pads on the chip to the single external ground lead. This technique also has the undesirable feature of bonding to a surface which is below the top surface of the chip. Another questionable area involves the supply voltage tunnel under the metalization between the two offset diodes and the base of the output transistors, and under the ground metalization. Additional wires and bonds and resistive tunnels are generally avoided unless absolutely necessary. Another method of handling this circuit is shown in Figure 7. This Motorola dual gate uses a 49 x 49 mil chip with aluminum metalization and one mil stitch bonded aluminum wire. In this case Motorola's ceramic package does not allow bonding ground leads to the package so they have increased the amount of metalization required for the ground connection and relied on a single wire to tie to the external ground lead. Note also the rather large area storage diode used as a speed-up capacitor across the

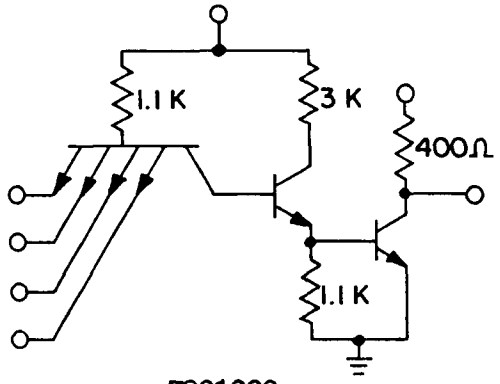


7901000

Motorola

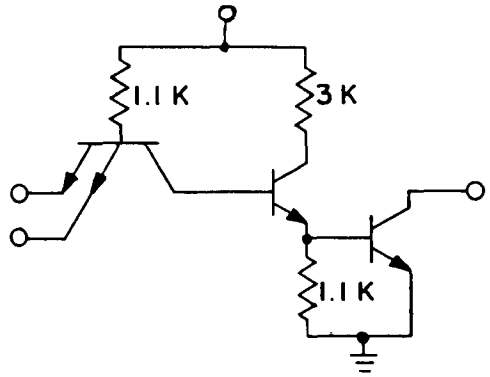


7901001

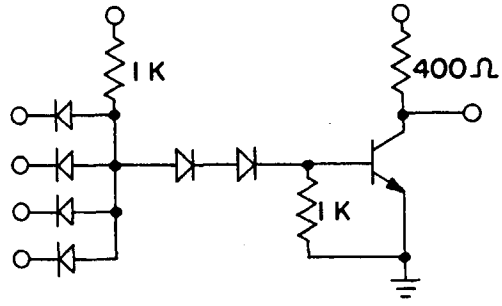


7901000

Signetics

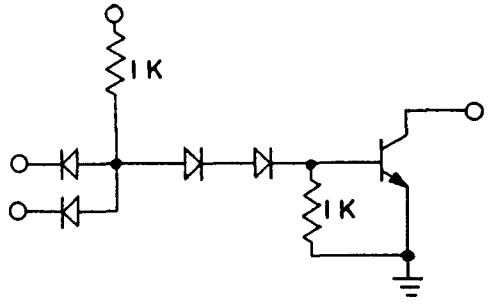


7901001



7901000

Westinghouse



7901001

(ONLY ONE GATE PER TYPE SHOWN)
VENDOR CIRCUIT CONFIGURATIONS

FIGURE 4

NOTE: All initial development orders placed during December 1965.

	Vendor	Status
1.	Fairchild	Cancelled 17 March 1965. Unacceptable electrical design. Very large speed-up capacitors.
2.	Signetics	Marginal prototypes delivered during March 1965. Partial cancellation 26 May 1965 due to inability to show future capability to meet specifications.
3.	Texas Instruments	Partial cancellation 12 April 1965. Inability to deliver electrically good units.
4.	Motorola	Marginal prototypes delivered from March through June 1965. Acceptable prototypes delivered in September 1965.
5.	Westinghouse	Acceptable duals delivered during March 1965. Acceptable quads delivered during April 1965. Majority of order delivered during May and June 1965.

FIGURE 5

offset diodes. The quad gate (7901001) which requires more individual components is a more striking example of the differences between the two manufacturers. Figure 8 shows a Westinghouse quad gate with two inputs per gate using a 51 x 60 mil chip. This is a very clean chip considering its complexity but again multiple ground leads (this time four from the chip to the case and one from the case to the external lead wire) and two supply voltage tunnels are required. Compare this to Figure 9 showing the Motorola quad gate on a 55 x 55 mil chip. Motorola is required to use a wide metalization path which surrounds 3/4 of the active area. When the long path used for the supply voltage metalization is included, it means that 10 of the 14 lead wires cross over metalization at some other voltage potential and that each is longer than normally required. Note again the four large storage diodes along a line through the center of the chip. It should be quite obvious that the optimum layout of a complex high performance monolithic chip involves trial and error, followed by compromise.

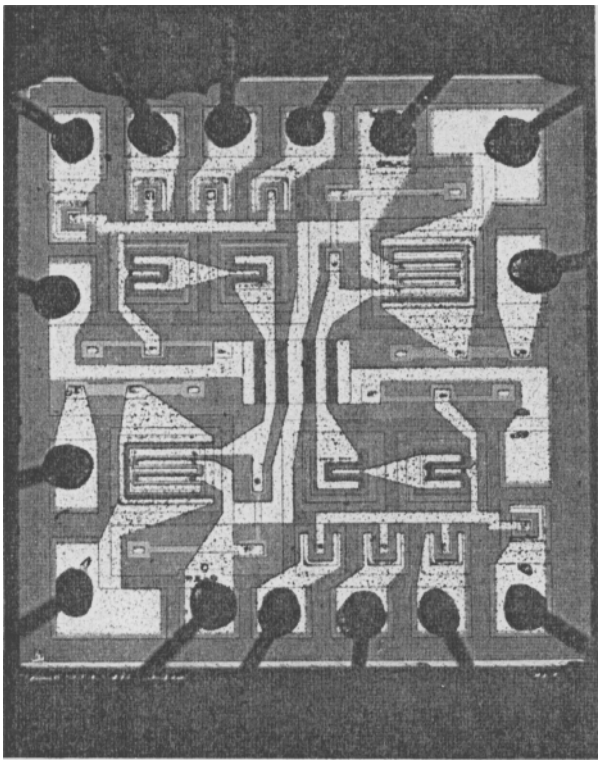


FIGURE 6

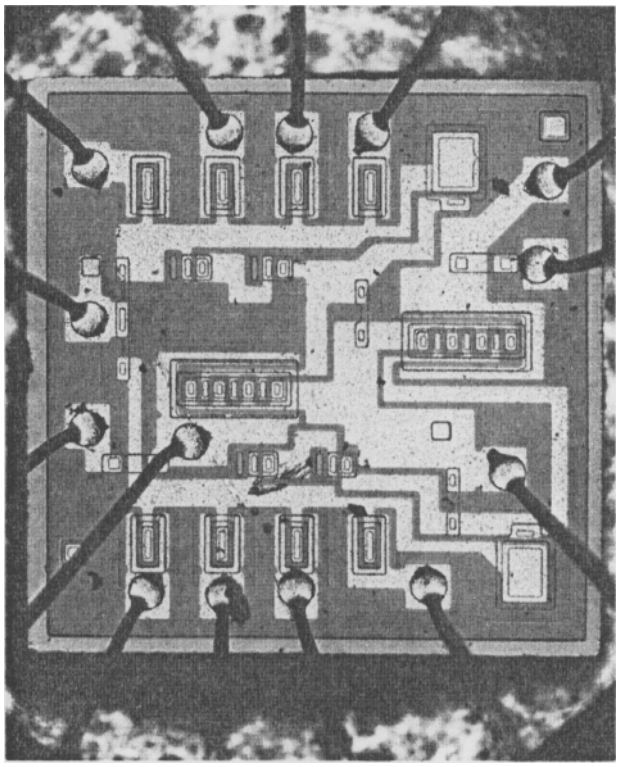


FIGURE 7

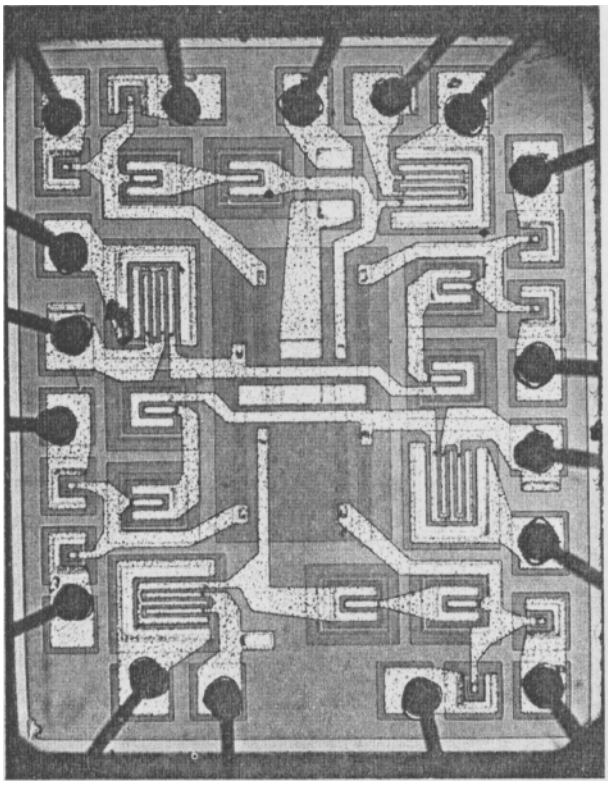


FIGURE 8

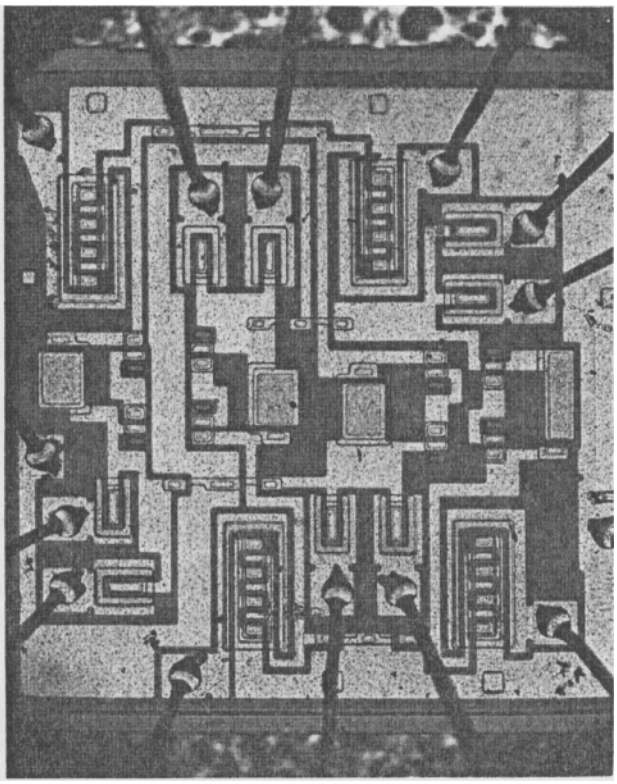


FIGURE 9

Since one of the major reasons for funding a custom design on this circuit family involved the need for a very fast logic circuit, it is important to discuss the test data which has been accumulated. As mentioned earlier, experienced engineers from both the Reliability and Design Engineering groups worked together on all phases of this development. The data taken was gathered by both of these groups. Figure 10 lists the nominal operating conditions for these two circuits. It is at this point that the major advantages and disadvantages of this circuit family should be apparent. The major advantages involve very high speed, high noise immunity over the entire MIL temperature range, the ability to perform collector logic (allowing two levels of logic to

Characteristic	"7901000"
1. Package	14 Lead Flat Pack
2. Fanout	6
3. Collector Logic Capability	Yes
4. Operating Temperature	-55°C to +125°C
5. Power Per Inverter (Avg.)	30 MW
6. Noise Margin (Minimum)	.35 V
7. Supply Voltages	6 V and 3 V
8. Propagation Speed (Typ.)	10 NS

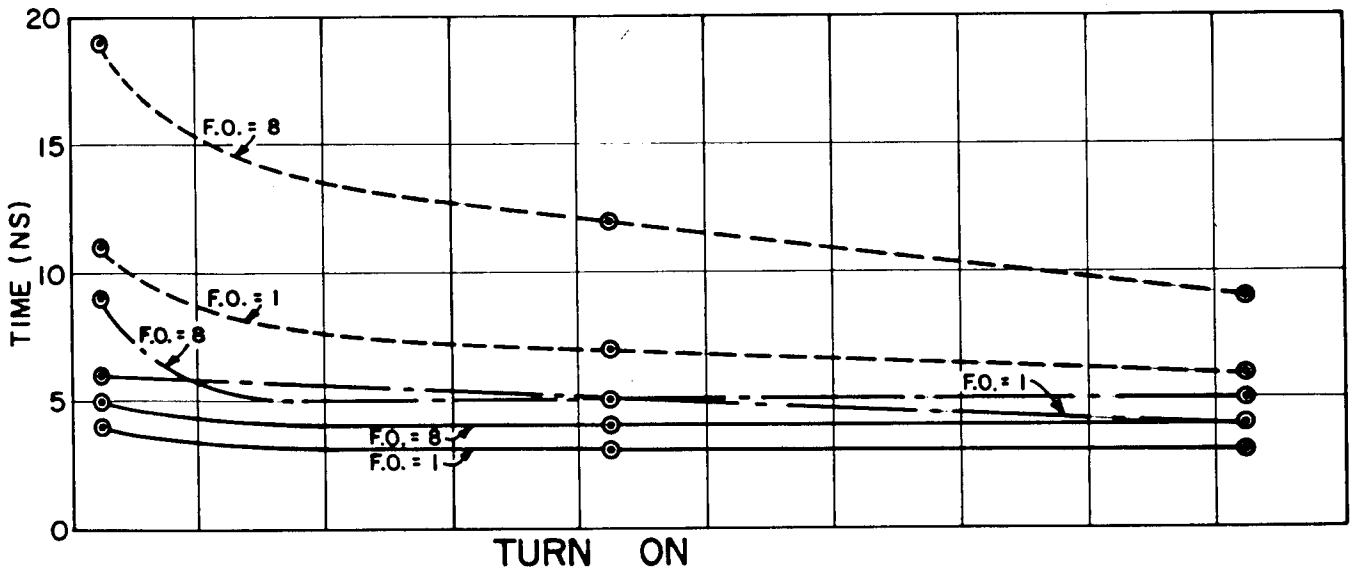
FIGURE 10

be performed in one propagation time) and potential low cost due to the straight forward layout possible. The primary disadvantage of the family is centered around the relatively high power dissipated in each gate. While power dissipation is critically important in most deep space and aerospace work, other considerations are more important for avionics, ground, and commercial applications. It is in these areas that this logic circuit is intended to excel. Because propagation times are normally given first consideration, Figure 11 plots a typical circuit under minimum and maximum loading at various supply voltages, against ambient temperature. Although the propagation times are quite low over most of the operating range, a storage phenomenon is evident at the highest supply voltage and operating temperature. Although this combination of conditions is not present in any of the systems now under consideration for these circuits, we are spending a great deal of time on this problem. It appears likely after lengthy discussions with our suppliers that process control offers the most promising solution. Process improvements that eliminate this storage effect at the voltage and temperature extremes, will also offer better control and possible improvement at normal operating conditions. A comparison between the propagation delay times under minimum and maximum loading for the basic logic gates used in our two preferred integrated circuit families (7901000 and 7900310) is shown in Figure 12. As explained earlier, the 7901000 originally developed for 667 was designed for maximum speed with dissipation a secondary consideration. The 7900310, on the other hand, stresses low dissipation at moderate speeds optimizing it for the 1824 aerospace computer.

SWITCHING SPEED FOR WESTINGHOUSE WS-282
7901000
MEASURED THRESHOLD TO THRESHOLD

V_T = 1.1 V @ +125°C
= 1.3 V @ + 25°C
= 1.6 V @ - 55°C

——— V_{SIG} = 7 V, V_L = 3 V, C_L = 20 pf
—·— V_{SIG} = 6 V, V_L = 3 V, C_L = 20 pf
------ V_{SIG} = 5 V, V_L = 3 V, C_L = 20 pf



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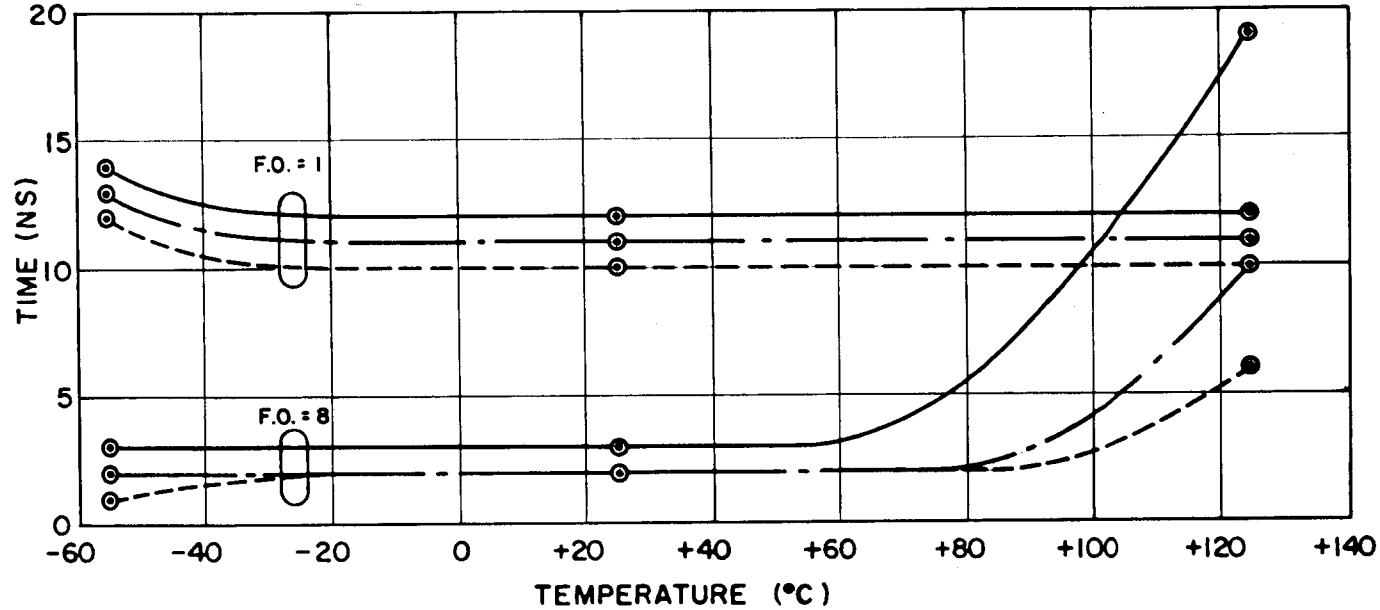

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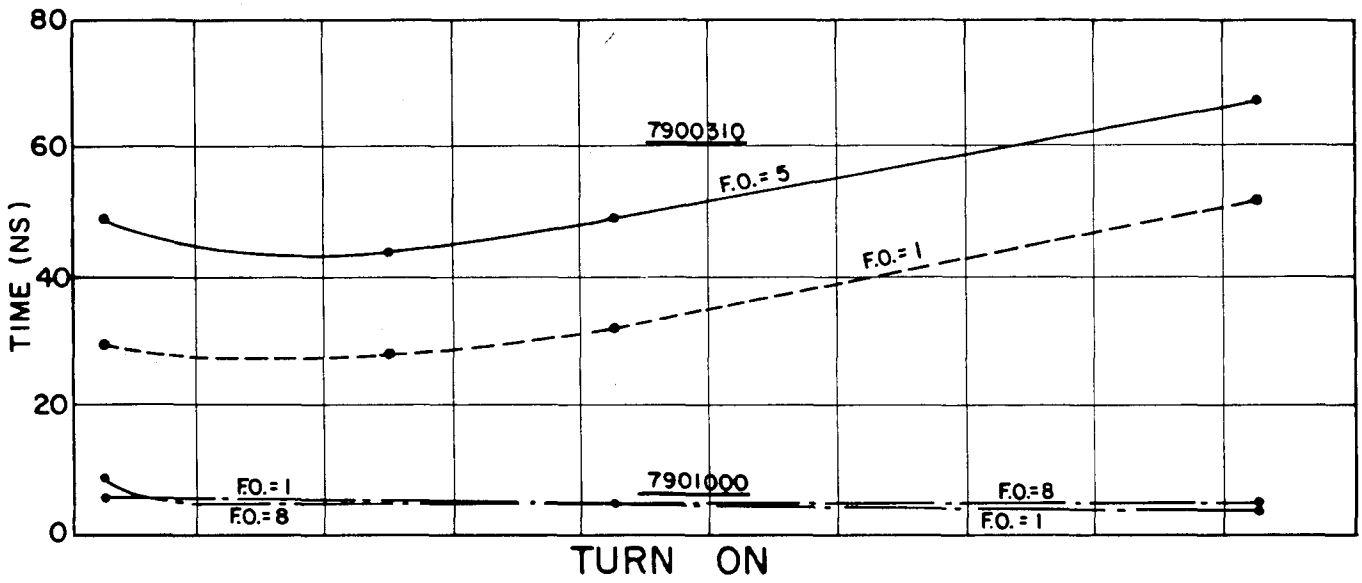
FIGURE 11

SWITCHING SPEED FOR WESTINGHOUSE 7900310 AND 7901000 MEASURED THRESHOLD TO THRESHOLD NOMINAL OPERATING CHARACTERISTICS

7900310	7901000
V_S = 4 V	V_{SIG} = 6 V
C_L = 50 pf.	V_S = 3 V
	C_L = 20 pf.

THE 7900310 IS SPECIFIED TO OPERATE FROM 0°C TO +125°C, WHILE THE 7901000 IS SPECIFIED TO OPERATE OVER THE FULL TEMPERATURE RANGE OF -55°C TO +125°C.



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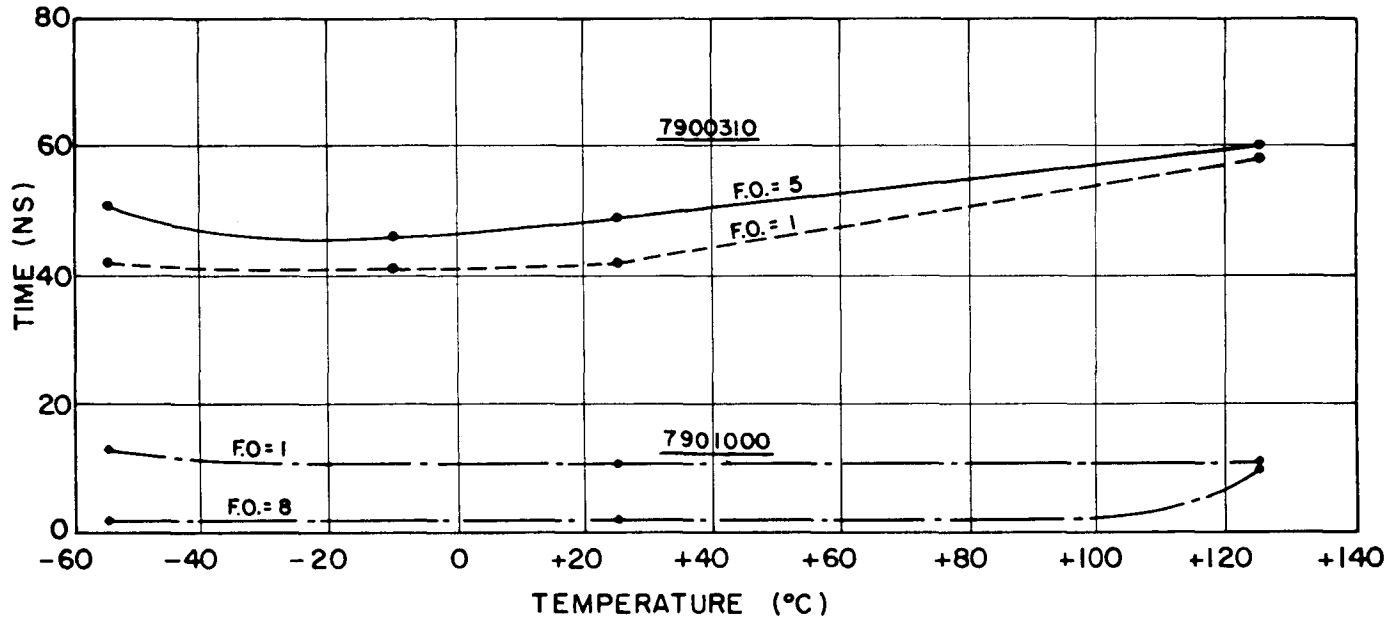

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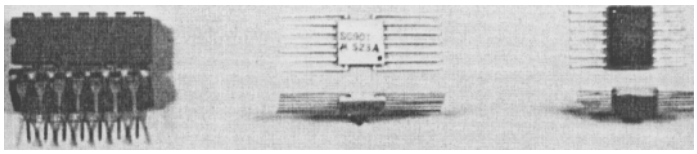
FIGURE 12

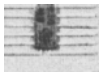
A major consideration involved in the application of integrated circuits involves the selection of the package. In order to better understand the various integrated, circuit packages which are being used at present, note the relative sizes shown in Figure 13. All four of the small flat packages (using ribbon leads on 50 mil centers) are being used interchangeably by St. Paul Defense while the larger package (with stiff leads on 100 mil centers) for plug-in applications is under development for Blue Bell commercial machines. Since



FAIRCHILD
1/4 "X 3 /4 "
DUAL IN LINE
PACKAGE
ALL CERAMIC

MOTOROLA
1/4" X 1/4"
FLAT PAK
ALL CERAMIC

SIGNETICS
1/4" X 3/8"
FLAT PAK
KOVAR LID
GLASS PACKAGE



T. I.
1/4"X 1/8"
FLAT PAK
KOVAR PACKAGE

WESTINGHOUSE
1/4" X 1/4"
FLAT PAK
KOVAR PACKAGE

MOTOROLA
0.350" DIA
10 LEAD-TO-5
KOVAR CAN
CERAMIC HEADER

FIGURE 13

virtually any monalithic chip currently under consideration by any of the three UNIVAC locations can fit into any of the 14 pin packages shown, standardization between locations at the chip level is being considered. Compromises are again involved in the selection of a preferred package similar to those discussed on chip layout. Each of the packages has its advantages and disadvantages in the following areas: cost, density, hermeticity, handling and availability. It is the writer's opinion that both basic types of packages will become industry standards (the smaller packages have already received JEDEC approval) for present 14 Pin circuit complexity. Even larger packages covering increasingly complex functional blocks are already being proposed for future applications.

As the usage of integrated circuits increases within UNIVAC, the need for accurate rapid measurement of each of the circuit parameters becomes increasingly important. Six years ago the Test Laboratory in St. Paul designed and built a large scale Automatic Component Tester (ACT) shown in Figure 14, for D.C. measurements on transistors and diodes. Because of the modular approach, extensive data output, complete suppression of transients, and extreme accuracy available within this machine, the ACT is presently being used virtually full time.

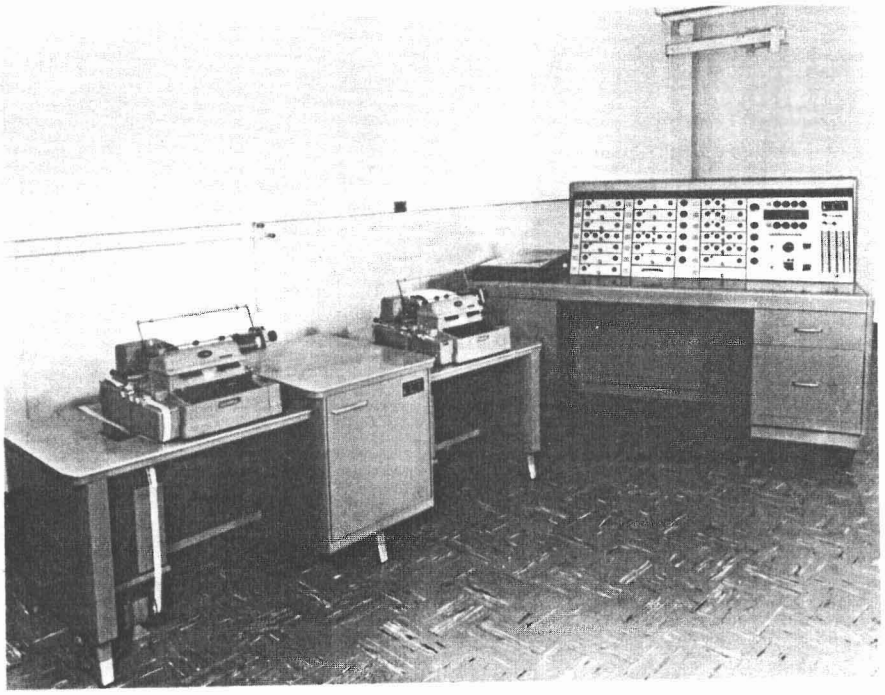


FIGURE 14

More recently, a special integrated circuit handler (shown in Figure 15) was built to tie in directly with the ACT measurement circuitry and data output. The handler uses special program cards on a large pin board to establish the measurement configuration. Fifteen different configurations are possible with a capability for three different measurements in each configuration. For example, one configuration might select a particular input diode on which forward voltage drop at a selected forward current and reverse leakage at two different reverse voltages is measured and recorded. The vertical axis on each card is used to select the desired combination of 14 pins on the circuit under test, while the horizontal axis applies the appropriate voltage or current and the necessary measurement circuitry. The handler automatically cycles through 10 measurement

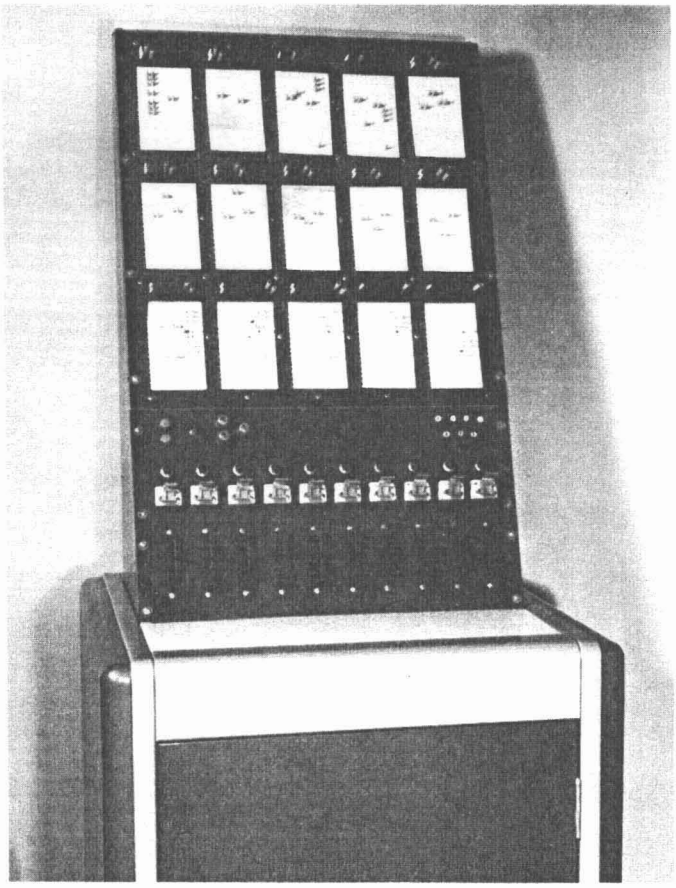


FIGURE 15

sockets in sequence taking all of the programmed readings on one device and then indexing to the next device. The handler, therefore, has a capability for a maximum of 45 parameters on each of 10 circuits at one loading. Fourteen pin Barnes sockets are used for flat paks while printed circuit connectors accept special boards for other packages. Once the handler is started, circuits can be loaded while measurements continue since all pins are shorted except when a measurement is being taken. An improved handler is now under construction allowing for twenty configurations or sixty measurements per device, and adding the desirable feature of potential sensing using separate voltage and current probes. While this arrangement is adequate for the present, significant improvements in A.C. measurement capability are needed immediately. A company funded design and development effort for such a tester is now underway. The program was started in early 1964 but did not swing into high gear until funding became available during the current fiscal year.

The tester, dubbed ACMET (A.C. Microelectronic Element Tester), consists of an automatic instrument package, a logic and input-output package, and a handler. The instrument package which is on order from Tektronix, consists of a programmable type 567 sampling scope, a wired card programmer unit, and a programmable pulse generator. It will have the capability to take measurements between two points on the same wave form or from a selected point on the input wave form to a selected point on the output wave form. Each point can be established independently at a given percentage of the wave form amplitude or at a discrete instantaneous voltage referred to ground or to a D.C. reference voltage. This allows it to be used to take virtually any switching or propagation time measurement. It also has the capability to measure D.C. voltages in much the same manner used in taking amplitude measurements. A.C. and pulse current measurements can be taken by installing current probes in the test circuit.

The logic control and input-output package which is being built by UNIVAC, will consist of the necessary registers and buffers and make use of standard NTDS printed circuit cards wherever possible. Program input will be from a paper tape reader while the output will be printed on a Flexowriter. A very desirable goal being considered during the present hardware design stage, involves an online interface with a 1218 computer. This would allow rapid calculation of distribution information, parameter shifts, and failure rate figures. Such a computer tie-up should offer a significant improvement in our ability to handle large amounts of data without delay.

The third and most difficult portion of the tester, involves the circuit handler. This handler must provide all necessary connections between the device under test and the measurement system. The handler must be capable of applying and switching the various supply, input, and output signals with a minimum of ringing. Since many of these measurements must be made at temperature extremes, various types of pedestals, controlled gas flow, and chambers are under investigation. The necessity of rapid loading and unloading dictates that some type of a carrier and feed mechanism be designed. Since the development work on the handler is still in its early stages, the final form it will take is not known.

While the A.C. tester is receiving top priority, a new D.C. integrated circuit tester having increased flexability, automatic handling, and temperature extreme capability, is under consideration for future requirements. Although

most of the D.C. receiving-inspection testing is now done on the test lab ACT, it is anticipated that a new tester will be built or purchased for large volume inspection purposes. The completion of the ACMET is presently planned for the second quarter of 1966 by which time development or delivery of the improved D.C. inspection equipment should be in its advanced stages.

A major phase of the development program on the 7901000 circuit family involves the qualification test being conducted by the Reliability Department. This test program is designed to assess the inherent reliability of these circuits and to environmentally stress them at those mechanical and electrical stress levels known to be indicative of adequate design margins, process controls, and workmanship. Step stress testing is included to indicate overload capability. The test conditions and levels were selected to detect the possibility of failure modes which have caused equipment problems with earlier discrete and partially integrated semiconductors. The test program which is now in process is shown in Figure 16. A total of 100 devices of each type from each vendor are on test. The 60 units compromising Group 1 and Group III go through the normal UNIVAC qualification tests used on all semiconductors except that several of the tests are run in parallel rather than sequentially. The 28 units in Group II are being tested to destruction on a high stress, short term step stress.

Although the qualification test is not complete, many of the tests on the Westinghouse circuits have been conducted. Figure 17 and 18 show the results obtained to date. Of primary concern during the early stages of the development program, was the ability of 7901001 to handle the dissipation of four gates at +125°C. The step stress results indicating no failures through +175°C ambient while dissipating full power, are quite encouraging. This test has been temporarily interrupted while we look for a method of attaching each circuit in a ring counter at ambient temperatures above 200°C. The printed circuit boards and soldered connections failed at 200°C although the circuits are still good. The temperature shock, hermetic seal, and mechanical tests conducted in Group I have looked good except for the two failure groups indicated. The single seal test failure found during the VEECO helium leak test, is a carryover from earlier days when package hermeticity was a serious problem. Since the measured leak rate on this unit was not excessive, the failure is not considered serious in itself. The four devices failing during 1500G mechanical shock are another story. Although this test is designed to produce opens in mechanically weak units, each of the units failed due to moderate values of leakage current which subsequently corrected itself several days later. These four units along with circuits from another test indicating a similar phenomenon, are presently included in a mysterious failure category which is receiving a careful analysis. We are attempting to determine whether these leakages are due to circuit weaknesses or to poor test techniques. Since the failure corrects itself, analysis obviously is quite difficult. The centrifuge step stress has progressed to 40,000 G without any failures. It is anticipated that we will go up to the maximum capability of the centrifuge--75,000 G. The temperature step stress reached 250°C before resistance and saturation voltage changes occurred and 300°C before catastrophic failures occurred. Surprisingly, two of the dual gates survived 400°C without catastrophic failure, although the leakages and saturation voltages are much higher than originally. The balance of the test sequence is now in process. Since only limited quantities of the Motorola circuits have been received, very little reliability testing has been conducted on them. It is anticipated that this testing will start in approximately one month.

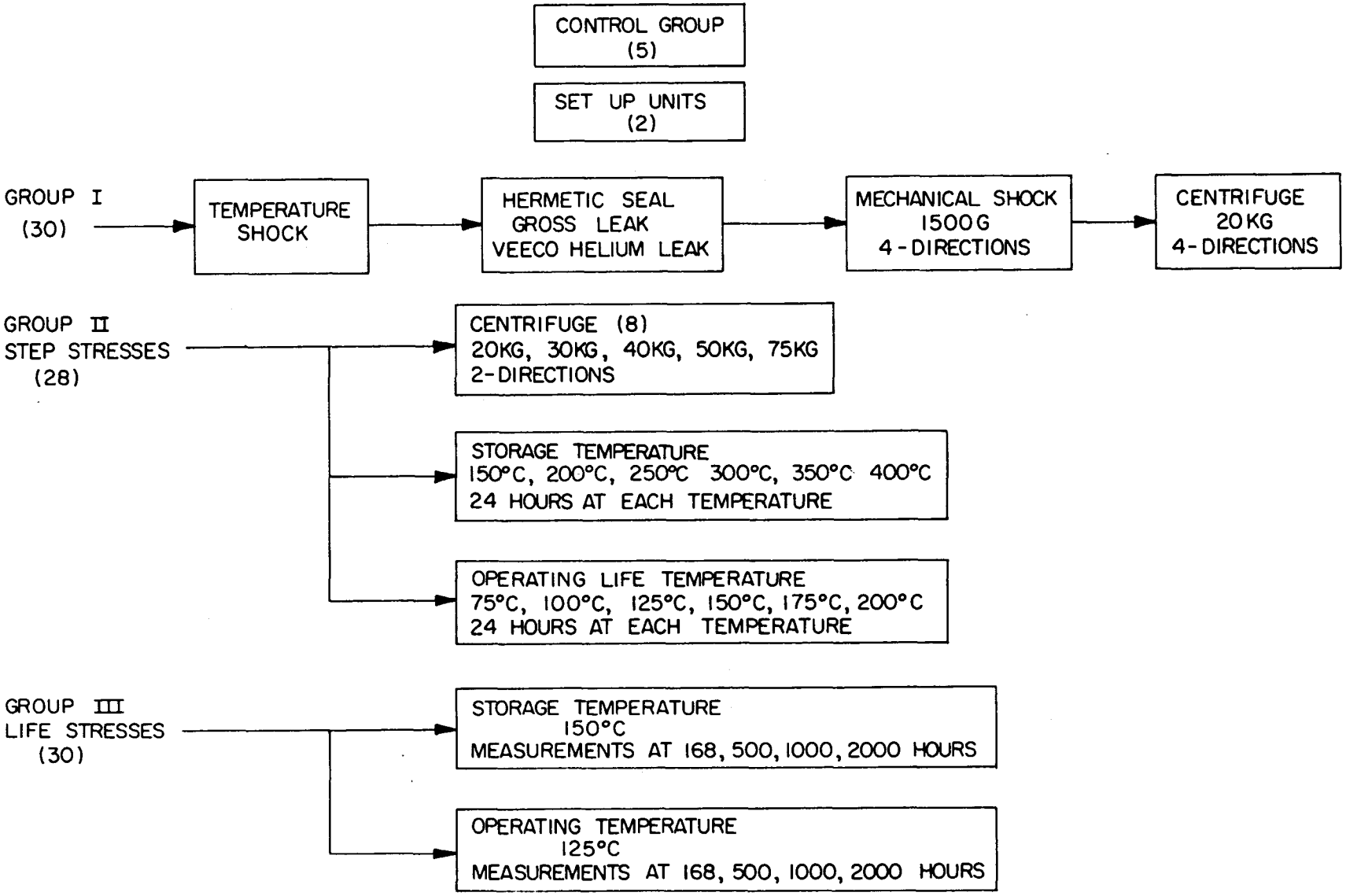

CONTROL GROUP
(5)
SET UP UNITS
(2)
GROUP I
(30)
TEMPERATURE
SHOCK
HERMETIC SEAL
GROSS LEAK
VEECO HELIUM LEAK
MECHANICAL SHOCK
1500G
4-DIRECTIONS
CENTRIFUGE
20KG
4-DIRECTIONS
GROUP II
STEP STRESSES
(28)
CENTRIFUGE (8)
20KG, 30KG, 40KG, 50KG, 75KG
2-DIRECTIONS
STORAGE TEMPERATURE
150°C, 200°C, 250°C 300°C, 350°C 400°C
24 HOURS AT EACH TEMPERATURE
OPERATING LIFE TEMPERATURE
75°C, 100°C, 125°C, 150°C, 175°C, 200°C
24 HOURS AT EACH TEMPERATURE
GROUP III
LIFE STRESSES
(30)
STORAGE TEMPERATURE
150°C
MEASUREMENTS AT 168, 500, 1000, 2000 HOURS
OPERATING TEMPERATURE
125°C
MEASUREMENTS AT 168, 500, 1000, 2000 HOURS

FIGURE 16

QUAL TEST RESULTS FOR WESTINGHOUSE

WESTINGHOUSE 7901000

GROUP I (30 UNITS)	TEMPERATURE SHOCK 0	GROSS LEAK 0	VEECO 0	1500G MECHANICAL SHOCK 2	CENTRIFUGE 20 KG 0	
GROUP II (28 UNITS)						
CENTRIFUGE STEP (8)	20KG Z1 0	20KG Z2 0	30KG Z1 0	30KG Z2 0	40KG Z1 0	
TEMPERATURE STEP (10)	150°C 0	200°C 0	250°C 0	300°C 1	350°C 2	400°C 5
OPERATING LIFE STEP (10)	75°C 0	100°C 0	125°C 0	150°C 0	175°C 0	200°C N.C.
GROUP III (30 UNITS)						
STORAGE TEMPERATURE (15 UNITS - 1 WEEK)	150°C 0					
OPERATING LIFE @ 125°C (15 UNITS - 1 WEEK)	125°C 0					

FIGURE 17

QUAL TEST RESULTS FOR WESTINGHOUSE

WESTINGHOUSE 7901001

GROUP I (30 UNITS)	TEMPERATURE SHOCK 0	GROSS LEAK 0	VEECO 1	1500G MECHANICAL SHOCK 2	CENTRIFUGE 20KG 0
GROUP II (28 UNITS)					
	20KG	20KG	30KG	30KG	40KG
CENTRIFUGE STEP STRESS (8)	Z1 0	Z2 0	Z1 0	Z2 0	Z1 0
TEMPERATURE STEP STRESS (10)	150°C 0	200°C 0	250°C 0	300°C 1	350°C 9
OPERATING LIFE STEP STRESS (10)	75°C 0	100°C 0	125°C 0	150°C 0	175°C 0
GROUP III (30 UNITS)					
STORAGE TEMPERATURE (15 UNITS - 1 WEEK)	150°C 0				
OPERATING LIFE @ 125°C (15 UNITS - 1 WEEK)	125°C 0				

FIGURE 18

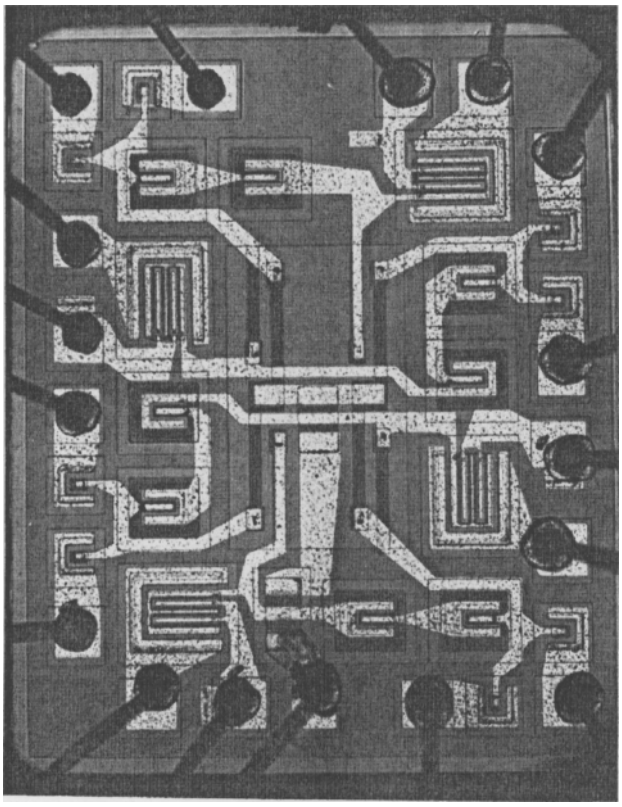


FIGURE 19

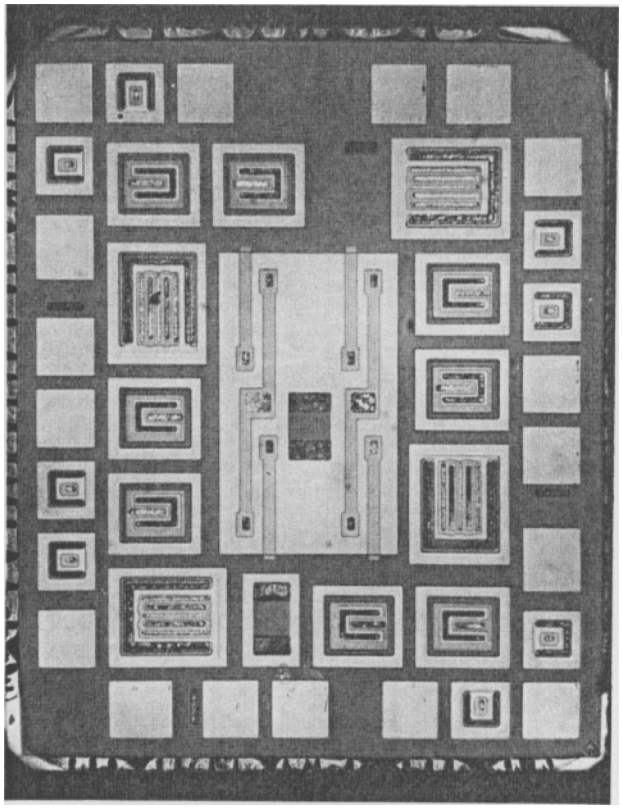


FIGURE 20

During the early phases of the development of these circuits, before enough circuits were available for the qualification test to start, extensive failure analysis was performed on each of the catastrophic failures found during receiving-inspection or electrical testing. Although very few such failures were found, the Defense Reliability Department places a great deal of emphasis on complete analysis of all failures. This is largely due to the quality of the people and facilities available for this work and because of the effective corrective action which results. The sequence of photographs shown in Figures 19, 20, and 21 follow the analysis of a Westinghouse 7901001 failure. This device found during receiving-inspection, developed a supply to substrate short circuit during high temperature testing. The first photograph of the original die clearly shows the over heated metalization adjacent

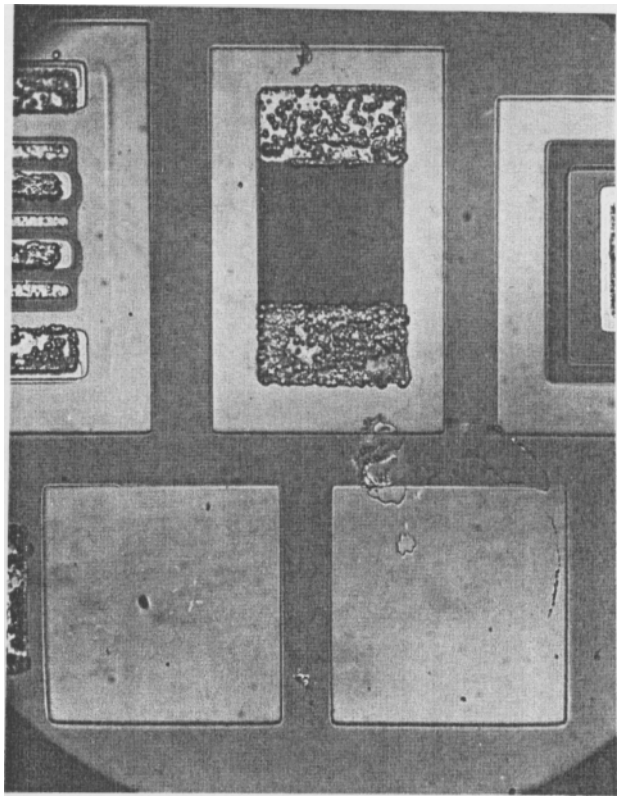


FIGURE 21

to the supply voltage bond. Although the natural conclusion would be to assume that failure was due to misuse (over voltage, wrong polarity, etc.) the second photograph with the bonds and aluminum metalization removed shows that the bond was misplaced, such that it missed part of the protective bonding tub provided. The third photograph, which is a close-up of the area involved, shows that too much pressure apparently caused the bond to break through the protective oxide passivating layer and short directly to the substrate. Localized heating resulting from the point contact short, along with insufficient current limiting in the test equipment, overheated the adjacent aluminum metalization. Although the sequence of events is not absolutely established in this case, the potential for corrective action available through complete failure analysis, should be apparent. A review of the test equipment limit circuitry was subsequently conducted at UNIVAC while the necessity of proper bond location and pressure was discussed with the vendor.

This paper has now developed in detail, much of the planning and techniques which go into the growth and final selection of a company standard integrated circuit family. The educational period necessary to develop the necessary understanding throughout the organization was mentioned. The engineering experimentation and calculations required to justify the selection of a particular class of circuitry were discussed. The necessity for enthusiastic cooperation between the various functional groups was stressed. The close contact required between the supplier and the user, necessary to obtain reliable high performance circuits was pointed out. The one point which I have not previously discussed, and the one which the writer feels personally has been more important to the success of this program than any other, involves management understanding of the technology involved and the complete support of management. While I agree with most of the people who are convinced of the fantastic promise of microelectronics, I am equally convinced that UNIVAC will be successful in this field only with wide spread standardization actively promoted by management. Progress and profits can be realized through well controlled, periodic updating of our circuits, but it has been well established that the cost of these circuits will be determined primarily by the volume per type which UNIVAC can commit at one time. Fortunately for the Reliability function which I represent, low cost, high volume circuits also offer the potential for optimum reliability.