

CP-642B COMPUTER
REPERTOIRE OF INSTRUCTIONS

UNIVAC

DIVISION OF SPERRY RAND CORPORATION

f01	Right Shift•Q	Shift (Q) Right by \underline{Y}
f02	Right Shift•A	Shift (A) Right by \underline{Y}
f03	Right Shift•AQ	Shift (AQ) Right by \underline{Y}
*f04	COMPARE•C ⁿ •AQ	Sense (j); $A_1 = A_f$
f05	Left Shift•Q	Shift (Q) Left by \underline{Y}
f06	Left Shift•A	Shift (A) Left by \underline{Y}
f07	Left Shift•AQ	Shift (AQ) Left by \underline{Y}
f10	ENTER•Q	$\underline{Y} \rightarrow Q$
f10	CLEAR•Q	$\underline{Y}=0, \underline{Y} \rightarrow Q$
f11	ENTER•A	$\underline{Y} \rightarrow A$
f11	CLEAR•A	$\underline{Y}=0, \underline{Y} \rightarrow A$
f12	ENTER•B ⁿ	$\underline{Y} \rightarrow B^j$
f12	CLEAR•B ⁿ	$\underline{Y}=0, \underline{Y} \rightarrow B^j$
f12	NO-OPERATION	Enter B ⁰ with 0 (do nothing operation)
^f13k0	EXTERNAL-COMMAND•C ⁿ •W(Y)•MONITOR	(Y) $\rightarrow C^j$; (interrupt at 00500+j)
^f13k2	EXTERNAL-COMMAND•C ⁿ •W(Y)	(Y) $\rightarrow C^j$
^f13k3	EXTERNAL-COMMAND•C ⁿ •W(Y)•FORCE	(Y) $\rightarrow C^j$; (to be used on all CP642A/USQ-20 peripheral equipment)
f14	STORE•Q	(Q) $\rightarrow Y$
f14k0	COMPLEMENT•Q	When Y is Q; then Q' $\rightarrow Q$
f15	STORE•A	(A) $\rightarrow Y$
f16	STORE•B ⁿ	(B) ^j $\rightarrow Y$
^f17k0	JUMP•Y•C ⁿ •COMACTIVE	Jump to \underline{Y} if external function buffer active
^f17k1	JUMP•L(Y)•C ⁿ •COMACTIVE	Jump to L(Y) if external function buffer active
^f17k3	STORE•C ⁿ •W(Y)	00520+j $\rightarrow (Y)$
^f17k2	STORE•C ⁿ •W(Y)•FORCE	Force C ^j $\rightarrow (Y)$ - (abnormal test mode)
f20	ADD•A	(A)+Y $\rightarrow A$
f21	SUBTRACT•A	(A)-Y $\rightarrow A$
f22	MULTIPLY	(AQ)/Y $\rightarrow AQ$
*f23	DIVIDE	(AQ)/Y $\rightarrow Q$; R $\rightarrow A_f$
*f23k7	SQUARE ROOT•Q	$\sqrt{ Q } \rightarrow Q$; residue $\rightarrow A$
f24	REPLACE•A•Y	(A)+(Y) $\rightarrow Y\&A$
f25	REPLACE•A-Y	(A)-(Y) $\rightarrow Y\&A$
*f26	ADD•Q	(Q)+Y $\rightarrow Q$
*f27	SUBTRACT•Q	(Q)-Y $\rightarrow Q$
f30	ENTER•Y•Q	$\underline{Y}+Q \rightarrow A$
f31	ENTER•Y-Q	$\underline{Y}-Q \rightarrow A$
f32	STORE•A+Q	(A)+(Q) $\rightarrow Y\&A$
f33	STORE•A-Q	(A)-(Q) $\rightarrow Y\&A$
f34	REPLACE•Y•Q	(Y)+(Q) $\rightarrow Y\&A$
f35	REPLACE•Y-Q	(Y)-(Q) $\rightarrow Y\&A$
f36	REPLACE•Y-1	(Y)+1 $\rightarrow Y\&A$
f37	REPLACE•Y-1	(Y)-1 $\rightarrow Y\&A$
*f40	ENTER•LP	L [Y(Q)] $\rightarrow A$
f41	ADD•LP	L [Y(Q)]+(A) $\rightarrow A$
f42	SUBTRACT•LP	(A)-L [Y(Q)] $\rightarrow A$
f43	COMPARE•MASK	(A)-L [Y(Q)] sense (j), A+L [Y(Q)]; (A) _i =(A) _f
*f44	REPLACE•LP	L(Y)(Q) $\rightarrow Y\&A$
f45	REPLACE•A+LP	L(Y)(Q)+(A) $\rightarrow Y\&A$
f46	REPLACE•A-LP	(A)-L(Y)(Q) $\rightarrow Y\&A$

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f02	Right Shift•A	Shift (A) Right by Y
f03	Right Shift•AQ	Shift (AQ) Right by Y
*f04	COMPARE•A•Q•AQ	Sense (j); $A_j = A_f$
f05	Left Shift•Q	Shift (Q) Left by Y
f06	Left Shift•A	Shift (A) Left by Y
f07	Left Shift•AQ	Shift (AQ) Left by Y
f10	ENTER•Q	$Y \rightarrow Q$
f10	CLEAR•Q	$Y=0, Y \rightarrow Q$
f11	ENTER•A	$\bar{Y} \rightarrow A$
f11	CLEAR•A	$\bar{Y}=0, \bar{Y} \rightarrow A$
f12	ENTER•B ⁿ	$\bar{Y} \rightarrow B^j$
f12	CLEAR•B ⁿ	$\bar{Y}=0, \bar{Y} \rightarrow B^j$
f12	NO-Operation	Enter BO with 0 (do nothing operation)
^f13k0	EXTERNAL-COMMAND•C ⁿ •W(Y)•MONITOR	(Y) $\rightarrow C^j$; (interrupt at 00500+j)
^f13k2	EXTERNAL-COMMAND•C ⁿ •W(Y)	(Y) $\rightarrow C^j$
^f13k3	EXTERNAL-COMMAND•C ⁿ •W(Y)•FORCE	(Y) $\rightarrow C^j$; (to be used on all CP642A/USQ-20 peripheral equipment) (Q) $\rightarrow Y$
f14	STORe•Q	When Y is Q; then $Q' \rightarrow Q$
f14k0	Complement•Q	(A) $\rightarrow Y$
f15	STORe•A	(B) ^j $\rightarrow Y$
f16	STORe•B ⁿ	Jump to Y if external function buffer active
^f17k0	JUMP•Y•C ⁿ •COMACTIVE	Jump to L(Y) if external function buffer active
^f17k1	JUMP•L(Y)•C ⁿ •COMACTIVE	00520+j $\rightarrow (Y)$
^f17k3	STORe•C ⁿ •W(Y)	
^f17k2	STORe•C ⁿ •W(Y)•FORCE	Force C ^j $\rightarrow (Y)$ - (abnormal test mode)
f20	ADD•A	(A)+Y $\rightarrow A$
f21	SUBtract•A	(A)-Y $\rightarrow A$
f22	MULtiply	(Q)Y $\rightarrow AQ$
*f23	DIVide	(AQ)/Y $\rightarrow R$; R $\rightarrow A_f$
*f23k7	SQuare Root•Q	$\sqrt{ Q } \rightarrow Q$; residue $\rightarrow A$
f24	RePLACE•A•X	(A)+(Y) $\rightarrow Y\&A$
f25	RePLACE•A•Y	(A)-(Y) $\rightarrow Y\&A$
*f26	ADD•Q	(Q)+Y $\rightarrow Q$
*f27	SUBtract•Q	(Q)-Y $\rightarrow Q$
f30	ENTER•X•Q	$X-Q \rightarrow A$
f31	ENTER•Y•Q	$\bar{Y}-Q \rightarrow A$
f32	STORe•A+Q	(A)+(Q) $\rightarrow Y\&A$
f33	STORe•A-Q	(A)-(Q) $\rightarrow Y\&A$
f34	RePLACE•Y•Q	(Y)+(Q) $\rightarrow Y\&A$
f35	RePLACE•Y•Q	(Y)-(Q) $\rightarrow Y\&A$
f36	RePLACE•Y ⁺¹	(Y)+1 $\rightarrow Y\&A$
f37	RePLACE•Y ⁻¹	(Y)-1 $\rightarrow Y\&A$
*f40	ENTER•LP	L [Y(Q)] $\rightarrow A$
f41	ADD•LP	L [Y(Q)] + (A) $\rightarrow A$
f42	SUBtract•LP	(A)-L [Y(Q)] $\rightarrow A$
f43	COMPARE•MASK	(A)-L [Y(Q)] sense (j), A+L [Y(Q)]; (A) _i = (A) _f
*f44	RePLACE•LP	L(Y)(Q) $\rightarrow Y\&A$
f45	RePLACE•A+LP	L(Y)(Q)+(A) $\rightarrow Y\&A$
f46	RePLACE•A-LP	(A)-L(Y)(Q) $\rightarrow Y\&A$

CP-642B COMPUTER REPERTOIRE OF INSTRUCTIONS

JP & RJP J-DESIGNATORS

j	JP f60	RJP f64	JP f61	RJP f65
0	(No Jump)*		(Uncond. Jump)	
1	(Uncond. Jump)*		KEY 1	
2	Q POS		KEY 2	
3	Q NEG		KEY 3	
4	A ZERO		STOP	
5	A NOT zero		STOP 5	
6	A POS		STOP 6	
7	A NEG		STOP 7	
8	62 j		63 j	
0-17 ₈	C ⁿ ACTIVE IN		C ⁿ ACTIVE OUT	

*60 Clears interrupt & bootstrap modes.

J - DESIGNATORS & K - DESIGNATORS

† Occupies 4 bit positions and represents Cⁿ where n may be 0-17₈.

‡ Controls operand interpretation, if it is limited to 2 bit positions since the †-designator requires 4 bits.

The instruction word assumes the format:

f † ‡ b y

29-	-24	23 - 20	19 18	17 - 15	14-	-0
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J - DESIGNATORS

j	COM•A, [*] Q, [*] AQ f04	DIV f23	ADD Q, SUB [*] Q f26	ENT•LP, RPL•LP f40	RPT f70	SQRT f23 k7
0	(no skip)	(no skip)	(no skip)	(no skip)	(no mod.); Y of NE = Y	(no skip)
1	(unconditional skip)	SKIP	SKIP	SKIP	ADV ; Y of NE = Y+1	SKIP
2	Y LESS : Y ≤ (Q)	NO OverFlow	A POS	EVEN parity	BACK ; Y of NE = Y-1	REM
3	Y MORE : Y > (Q)	OverFlow	A NEG	ODD parity	ADD B ; Y of NE = Y+B ⁶	NO REM
4	Y IN : (Q) < Y AND Y > (A)	A ZERO	Q ZERO	A ZERO	Rpl. Inc. ; Y of NE = Y[B ⁶] ✓ 'not used'	
5	Y OUT : (Q) < Y OR Y ≤ (A)	A NOT zero	Q NOT zero	A NOT zero	ADV R ; Y of NE = Y+[L,B ⁶] ✓ 'not used'	
6	Y LESS : Y ≤ (A)	A POS	Q POS	A POS	BACK R ; Y of NE = Y-[L,B ⁶] ✓ 'not used'	
7	Y MORE : Y > (Q)	A NEG	Q NEG	A NEG	ADD B R ; Y of NE = Y+B ⁶ [S,B ⁶] ✓ 'not used'	

✓ B⁶ Increment if NI is RPL class; increments Y address for the store portion of the replace.

NE - Next execution

NORMAL J - DESIGNATORS

j	Not applicable on * or ^)
	Skip Code
0	(no skip)
1	SKIP
2	Q POS
3	Q NEG
4	A ZERO
5	A NOT zero
6	A POS
7	A NEG

NORMAL K - DESIGNATORS

k	READ		STORE		REPLACE		
	Code	Origin	Code	Dest.	Code	Origin	Dest.
0	'blank'	U _L	Q	Q	'not used'	-	-
1	L	M _L	L	M _L	L	M _L	M _L
2	U	M _U	U	M _U	U	M _U	M _U
3	W	M	W	M	W	M	M
4	X	XU _L	A	A	'not used'	-	-
5	LX	X _M _L	CPL	CPL M _L	LX	X _M _L	M _L
6	UX	X _M _U	CPL	CPL M _U	UX	X _M _U	M _U
7	A	A	CPW	CPL M	'not used'	-	-

LEGEND

- M - Memory word (30 bits)
- M_L - Lower half memory word
- M_U - Upper half memory word
- X - Sign bit extended
- CPL - Complement
- A - A-register
- Q - Q-register

CP-642B MEMORY ADDRESS ASSIGNMENT

OCTAL ADDRESS RANGE	USE
00000 - 00000	Fault Entrance Address (With AUTOMATIC RECOVERY switch in center position) — illegal instruction code or illegal use of control memory
Core Memory 00001 - 00017 00020 - 00037 00040 - 00057 00060 - 00077	Unassigned External Interrupt Entrance Addresses Input Monitor Interrupt Entrance Addresses Output Monitor Interrupt Entrance Addresses
Control Memory 00100 - 00117 00120 - 00137 00140 - 00157 00160 - 00180 00161 - 00167 00170 - 00177	Input Buffer Control Words Output Buffer Control Words External Function Buffer Control Words Real-Time Clock B-Registers Unassigned
Core Memory 00200 - 00477 00500 - 00517 00520 - 00537	Unassigned External Function Buffer Monitor Interrupt Entrance Addresses Interrupt Word Storage Address
00540 - 00577	Bootstrap - Wired Memory
Core Memory 00600 - 00617 00620 - 77777	Intercomputer Time Out Interrupt Entrance Address Unassigned

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