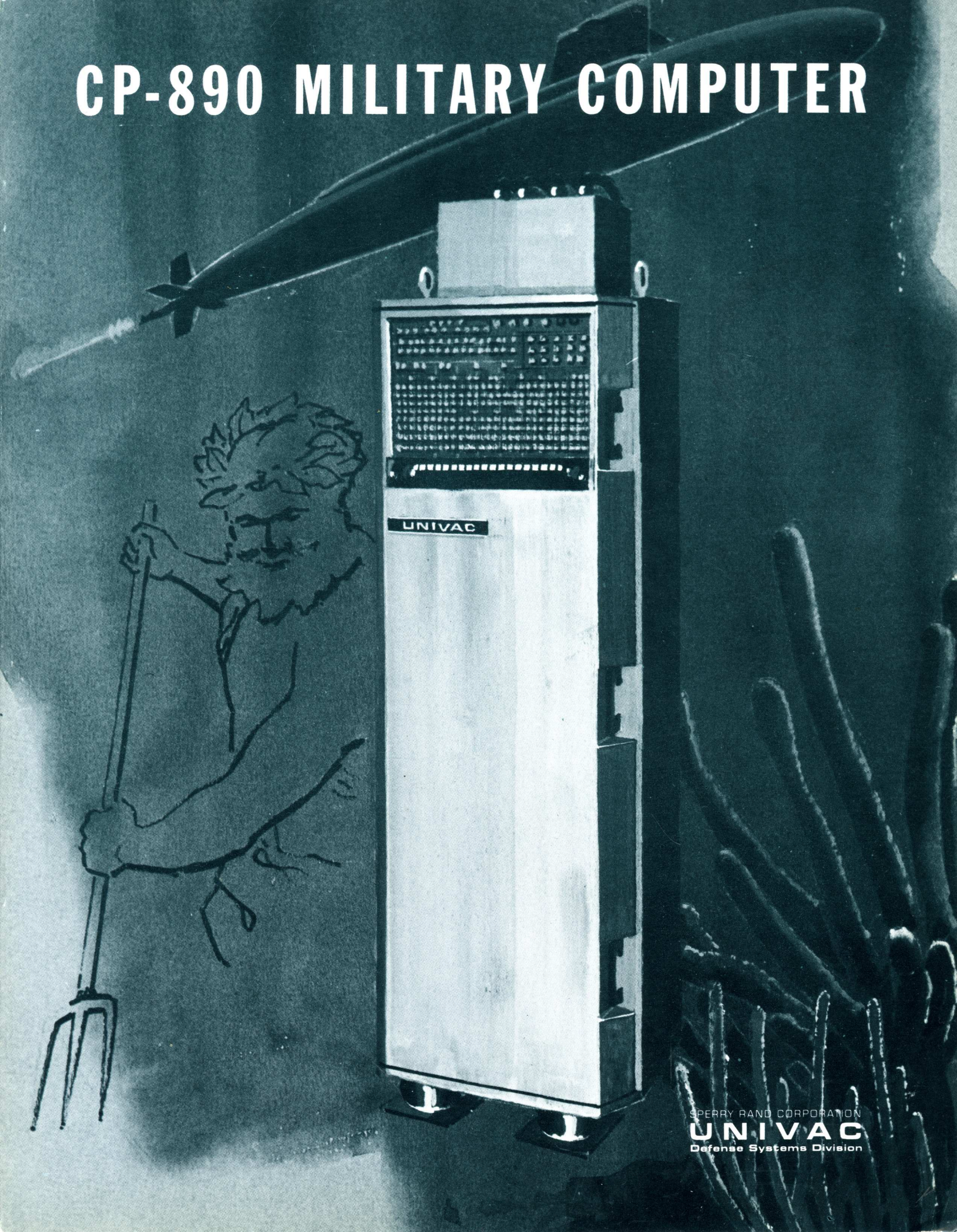
CP-890 MILITARY COMPUTER



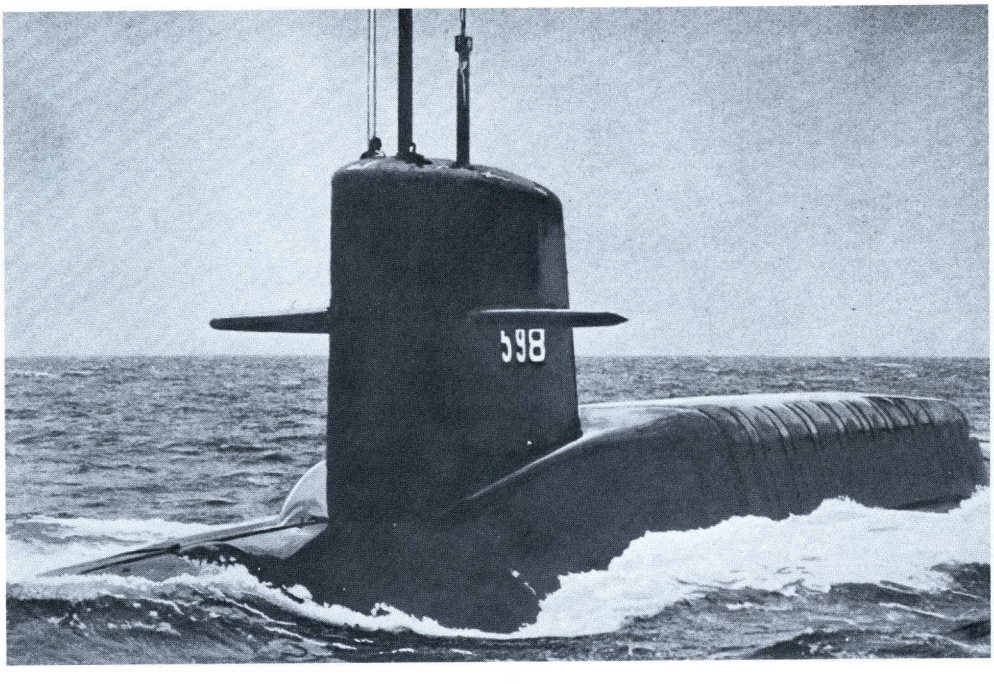
SPERRY RAND CORPORATION
UNIVAC
Defense Systems Division

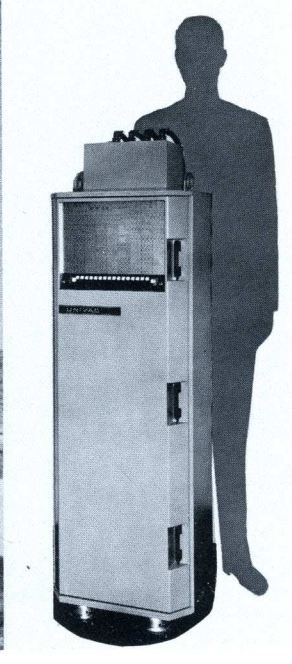
CP-890 MILITARY COMPUTER

INTRODUCTION

The advent of the nuclear submarine heralded a new and challenging era in Naval history. Travelling faster underwater than most surface ships, having unlimited range of operation, and possessing a formidable array of armament, the nuclear submarine unquestionably represents a powerful defensive and offensive weapons system.

In common with other Navy craft, nuclear submarines must resolve many problems in the course of the missions they undertake. These include navigation, ship control, fire control and other functions that constitute normal operation. The normally complex navigation problem of all vessels becomes magnified tenfold in a submarine. Modern ships use Loran, sextants, radar, or other aids to navigation but submarines must also rely on transit satellites and inertial guidance as well, for positioning when normal means are not feasible.

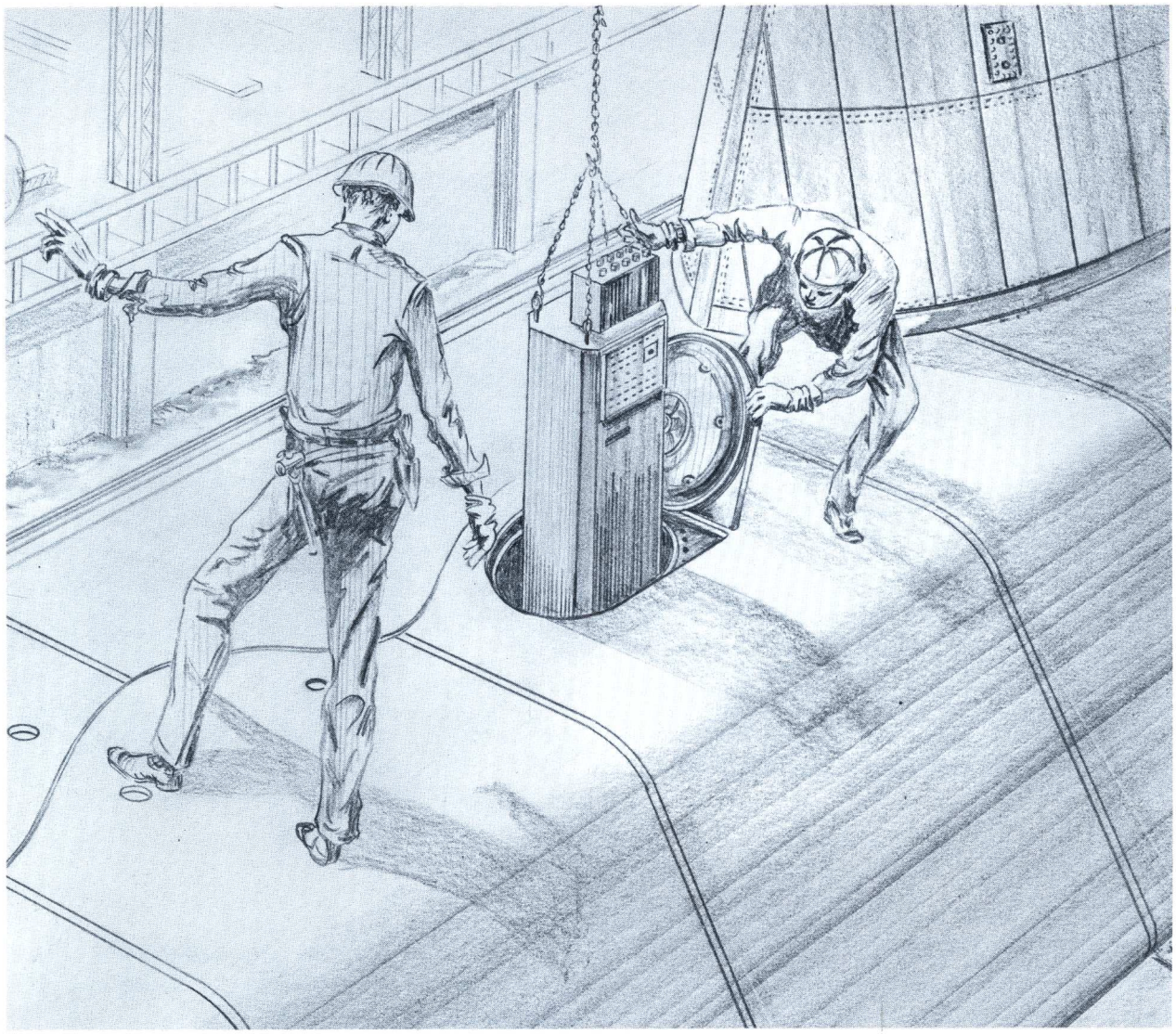


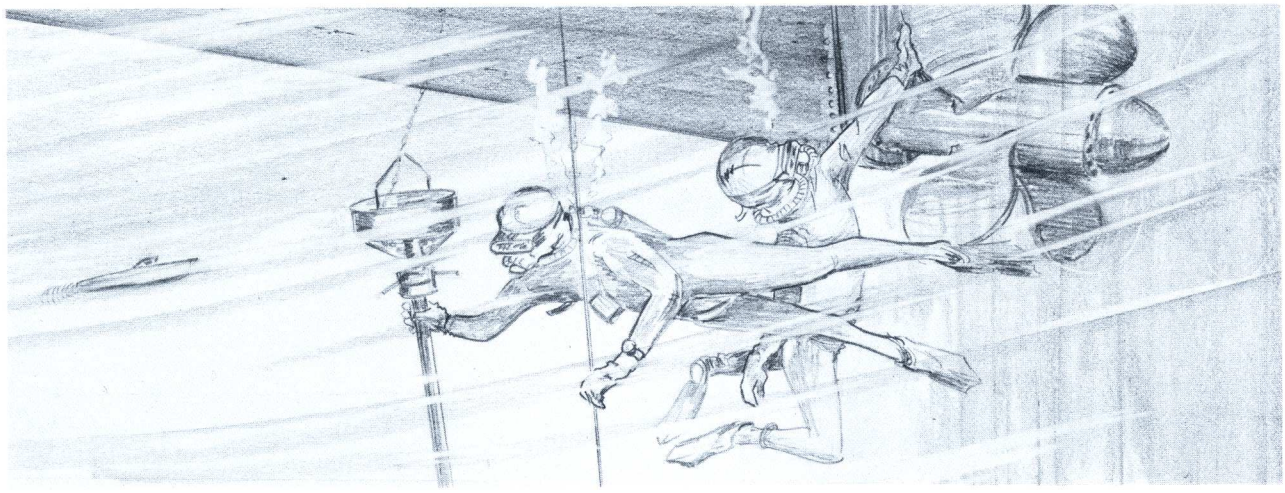


Mistakes in navigation or miscalculations in data computations cannot be tolerated. Obviously, navigation methods and techniques must be precise and swift. It is equally clear that such precision and speed impose impossible demands upon the personnel aboard ship—demands that exceed human capability.

UNIVAC has designed and built the CP-890 computer to satisfy the navigation requirements of the U. S. Navy's *Polaris* submarines. The Special Projects Office of the U. S. Navy sponsored the development of this computer. Under Navy Contract NObs 94306, the Sperry Rand Corporation's Sperry *Polaris* group and UNIVAC Defense Systems Division worked to answer this need.

The CP-890 is built to pass through a 25-inch diameter hatch without dismantling; weight and power were minimized while still providing general-purpose capability and applications. High card commonality with companion equipments yields low cost of ownership. The computer, because of its general-purpose nature, will greatly increase the effectiveness of any shipboard system in which it is used.





APPLICATIONS

A list of possible applications includes the following:

- Command and Control
- Navigation
- Integrated Submarine Systems
- Fire Control Systems
- Digital Communication
- Data Reduction and Analysis
- Simulation
- Sonar Signal Processing-Signal Enhancement
- Tactical Control
- Oceanographic Data Analysis, Retrieval, Display
- Weapon Direction
- Guidance
- Sensor Control.

SUMMARY

Weight: Approximately 650 pounds

Power: 3 phases, 400 cycles, 115 vac, 2000 watts

Functional Characteristics:

Memory—1.8 microseconds, 32K, 32 Bits
Overlapped
Asynchronous
2 parity bits
Expandable to 262K

Arithmetic—30 bits parallel, one's complement subtractive

Add time—1.8 microseconds

Multiply Time—7.2 microseconds

Input/Output—12 Input/Output Channels, Expandable to 16 Channels
Control Memory for Buffer Control Words
Intercomputer Capability

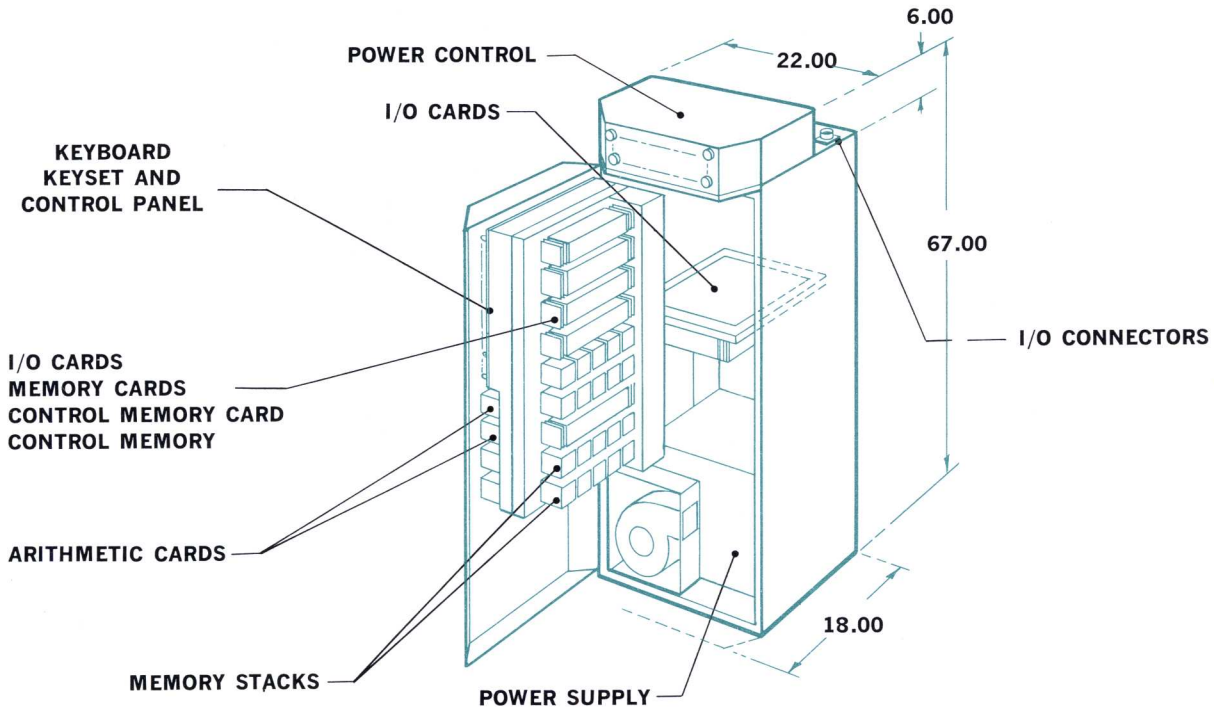
Index registers—7

Bootstrap—NDRO Memory for Initial Load and Automatic Recovery

PHYSICAL DESCRIPTION

The UNIVAC CP-890/UYK Military Computer has been designed and constructed to the exacting standards of MIL-E-16400 and MIL-I-983. The proven reliability of predecessor UNIVAC computers has been enhanced in the CP-890 Computer by the utilization of microelectronic circuitry and wire-wrapped connectors.

The physical configuration consists of two hinged chassis containing printed circuit logic cards and core memory array stacks. The computer cabinet is a NAV Type 1 module as shown in the figure. The cabinet measures 67 inches high, 22 inches wide, by 18 inches deep with chamfered corners designed to permit passage through a 25-inch diameter opening. A display panel includes approximately 400 indicator light switches, a keyboard, and a keyset. An internally contained blower cools the computer. The power supply is housed at the lower rear of the cabinet. The additional memory in excess of 32K words requires a separate cabinet.



UNIVAC CP-890/UYK MILITARY COMPUTER

The UNIVAC CP-890 Military Computer possesses many unique and outstanding features that make it especially effective when functioning in the applications previously mentioned. Some of these features are as follows:

- 32K words of memory
- 30-bit word length—instructions and operands
- Convenient processing of half-word operands
- Instruction repertoire oriented toward programming military problems (see Repertoire of Instructions)
- Seven index registers
- Internal real-time clock—under program control

- Repeat instruction—eliminates many program loops
- Input/output interface compatibility with many types of available peripheral equipment
- Intercomputer communication permits multiple configurations of UNIVAC military computers
- Asynchronous input/output and arithmetic operation
- External and internal interrupts provided on all input/output operations
- NDRO initial input and automatic recovery routines
- CS-1 compiler and an extensive group of library routines
- 12 input and 12 output channels
- Small volume—15 cubic feet
- Light weight—650 lbs.
- Split main memory with independent access to each 16K word memory bank
- Increased memory speed—effective cycle time of 900 nanoseconds with overlapped memory references
- Parity on each main memory half word
- Increased processing speed
- Double-precision, fixed-point operations
- Complete set of floating point instructions
- Direct, on-line interface between operator and program under execution, either local or remote
- Break-point feature
- Alarm clock associated with the real-time clock
- Provision for connecting an external real-time clock
- Power failure detection and protection
- Independent access to memory for processor and input/output
- Optional priority order on input/output channels
- Externally specified indexing mode of input/output operation
- Externally specified addressing mode of input/output operation
- Continuous data mode of input/output operation
- Fast input/output information transfer
  167 kc (single channel)
  500 kc (total interface)
- Discrete function external interrupts
- Advanced SYCOL compiling system
- Diagnostic maintenance procedures isolate malfunction to the least replaceable unit
- Programmable status or machine state register.

Because the computer reflects highly advanced design concepts, provision was made for system expansion, if desired, both in memory and in program organization and sophistication. For example, the computer contains the necessary logic and wiring to permit memory expansion to a maximum of 262 K words; it has a set of special instructions that provide an executive mode of operation; it features indirect addressing; and its input/output capability may be expanded to 16 input and 16 output channels.

FUNCTIONAL DESCRIPTION

Main storage consists of two 16K-word, ferrite-core banks, each independently accessible. In a 1.8-microsecond period, a memory reference can be completed in each bank, giving an effective speed of 1.1 megacycle. Separate paths to and from each memory bank are provided for instruction, operand, and input/output transfers. During periods of heavy input/output activity, one memory bank can be given to input/output for relatively exclusive use. During periods of light input/output activity, one bank can be used for instruction reference and the other bank for operand storage, thereby achieving overlapped program use of the memory. Consecutive addresses are contained in the same memory bank. All memory words are 32 bits long, permitting a parity bit for each 15-bit half word of information. A parity failure on a memory reference will initiate a special sequence within the computer to isolate the problem; after which, program control will be transferred to an interrupt program for interpretation and appropriate action. An accidental memory failure will be handled in a similar manner.

A special 64-word control memory is used primarily as input/output control registers. These locations are integral with the main memory addressing to permit their use as normal storage cells (in addition to having special significance).

A second special storage facility consists of 128 words of fixed memory for initial input and recovery programs (bootstrap).

Arithmetic and logical operations are performed in a parallel, binary mode. One's complement subtractive arithmetic with a modulus of $2^{30}-1$ is utilized. The repertoire of the basic instructions and those provided to enhance the computing power and versatility is given in the table with execution time. Representative instruction speeds are:

- Multiply— 7.2 microseconds
- Divide— 12.6 microseconds
- Square Root— 7.2 microseconds

Double-precision, fixed-point instructions provide for additional numerical significance. When used with the normalize instruction, efficient multiple-precision, floating-point subroutines can be developed. A special instruction is provided for sensing arithmetic overflow conditions.

The floating-point instruction set provides for a 30-bit mantissa, including sign, and a 15-bit characteristic, including sign, packed as a two-word pair. Both rounded and unrounded floating-point can be performed. Interrupts are provided to indicate characteristic overflow and underflow conditions.

The *Display Register* (30 bits) provides a man/machine interface through which an operator can communicate directly with the program being executed by the processor. Associated with the *Display Register* is a Test and Control (T/C) panel. Included on the panel are:

- Local Keyset
- Local Keyboard
- Remote/Local Control Switch
- Controls for Automatic Memory Load
- Displays for Internal Registers
- Controls for Computer Test and Diagnosis

The T/C panel obtains processor attention via an interrupt. The responding program in the processor will scan the *Display Register* for possible input data using the Sample Keyboard/Keyset and Store Display Register instructions. A program response to an external request will utilize the Enter Display Register instruction.

The *Break-point Register,* which can be addressed manually or by program, is used to identify an address of significance. Whenever this same address is used in an operand reference, an interrupt signals the occurrence.

Real-time programming is assisted by a clock monitor and a clock location in memory. The monitor location can be set to any value by an instruction. When the monitor location has been decremented to zero, an interrupt occurs. The real-time clock source can be either internal or external to the processor. The internal real time source is also available for external use as a system timing device.

Guard circuits are employed to detect abnormal fluctuations in supply power and to initiate an orderly programmed termination of processor activity. The operating power range is divided into a normal band and upper and lower peripheral bands. In a power failure, the inherent delay in the power drop through the lower peripheral band is sufficient to permit execution of a special instruction sequence to effect a controlled stop. Under these conditions, the validity of the program and machine status is assured, and on restoration of power, program control is transferred to a special restart instruction sequence.

A *Status Register* (30 bits) is used to define the state of the computer as it affects programming. Bit groupings or fields of the register serve as designators and indicators of interest to the program. Instructions are provided to load and store the *Status Register.*

An expanded repertoire of instructions represents built-in capability for a more comprehensive system. Special instructions, defining an executive mode of operation, are included in the expanded repertoire. These instructions are intended primarily for use by machine-oriented programmers (i.e., those responsible for program control, interrupt handling, input/output control, and on-line programmed testing). Each of these types of programs requires special sequences and procedures and places a premium on program efficiency.

Indirect addressing is provided by a special 7-bit designator in the *Status Register.* Each bit of the designator identifies an *Index Register.* If the designator for an *Index Register* is set and an instruction refences that *Index Register,* a special indirect addressing sequence is used in the execution of the instruction.

The input/output section is completely independent of the processor and is provided with a separate path to and from memory. The program merely activates it and supplies the proper initial parameters.

Priority in the input/output section is based on the type of service requested and the channel number of the request. A fixed association often develops between a peripheral device and a channel number. The principal need for altering this association arises from the necessity of changing the relative priorities of the various peripheral devices. The UNIVAC CP-890 Computer design permits reassignment of channel priorities, thereby eliminating this difficulty.

Supplementing the normal buffer modes of input and output operation other special modes are provided for greater flexibility in system applications. These standard features of the Computer are:

- Externally Specified Index (ESI)
- Externally Specified Address (ESA)
- Continuous Data Mode (CDM)
- Intercomputer Communication

The ESI mode permits a single channel to service many peripheral devices, each of which transmits to the input/output section, when requesting service, an identifier that is actually an index address in memory. This index defines the area in core memory that is reserved for the information transferred to or from the device.

The ESA mode permits each peripheral device on a channel to specify a single memory location involved in the storage or retrieval of data. The device specifies the absolute address when it requests service for input or output.

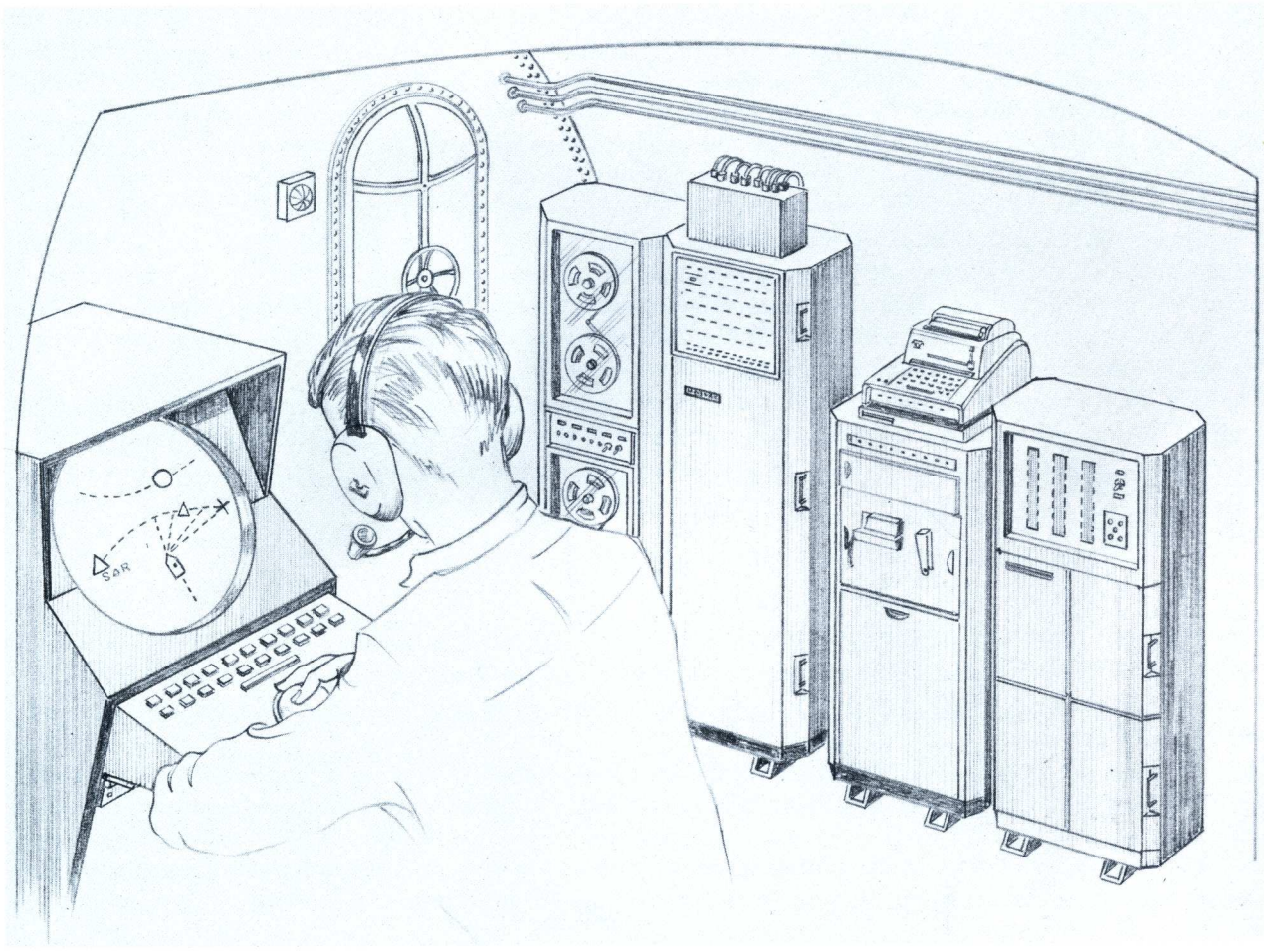
Either the ESI or ESA Mode can be selected as an alternate to the normal buffer operation for each input and output channel pair, thereby adding versatility to meet system requirements.

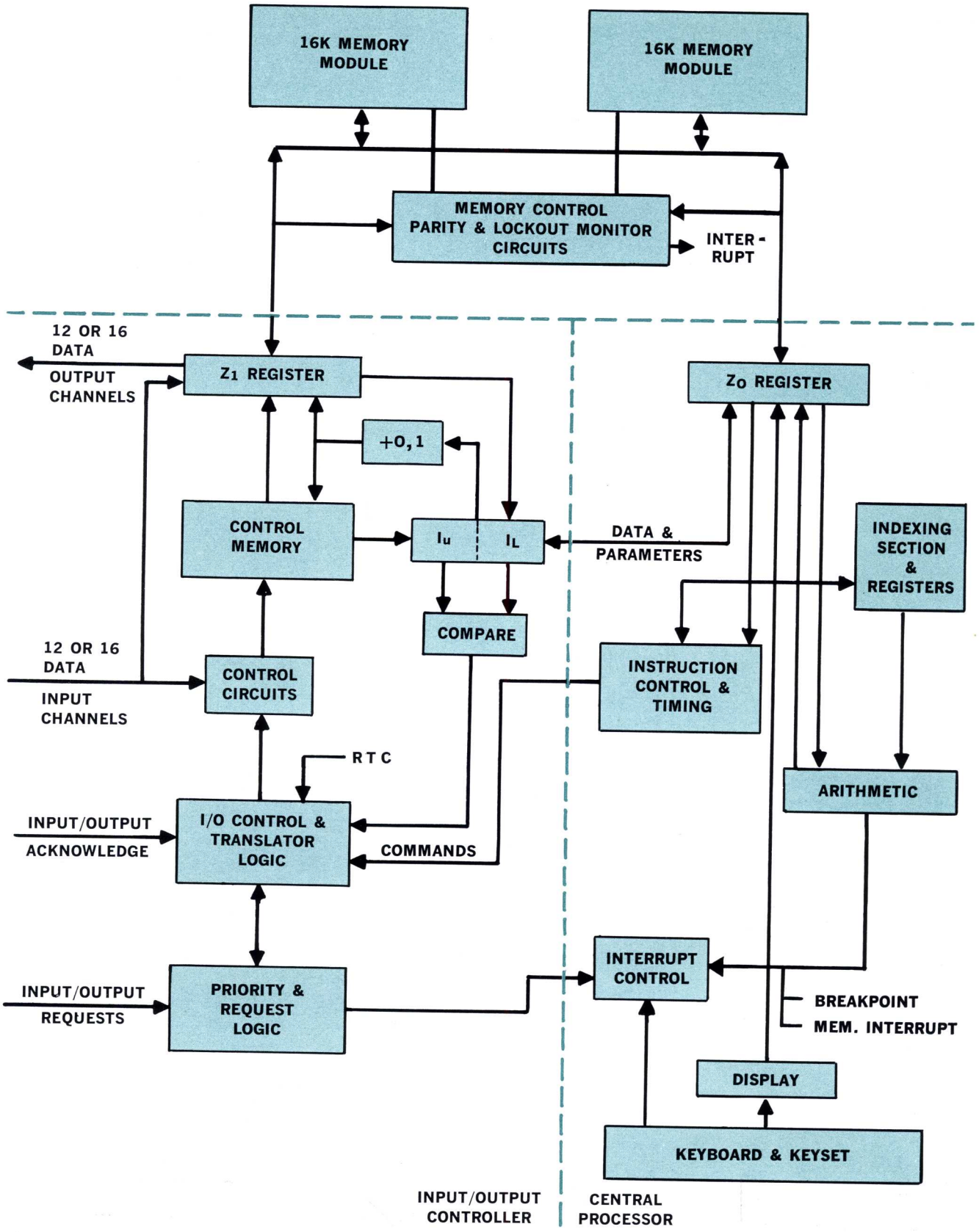
The CDM permits automatic reinitiation of an input or output buffer upon a previous completion. After the program establishes the CDM on a selected channel, the input/output section executes the process. A special reload location contains addresses that define another (or the same) buffer area. When the active buffer terminates, these addresses are transferred, without program attention, to the control location for the channel, and the buffer is reactivated. If successive buffers are to involve different areas of memory, it is a program responsibility to change the contents of the reload location each time.

Any channel that requires communication with another UNIVAC computer in a system can be assigned the intercomputer functional characteristic. The ESI, ESA, and intercomputer features are provided by simple plug-in type wiring changes and can be done at the computer site.

The input/output section can be equipped with either fast channels (167 kc) or slow channels (40 kc) in groups of four. Normally, the UNIVAC CP-890 Computer is delivered with 12 input/output channels, but 16 input/output channels are wired into the main frame.

Each input channel is allowed the capability of interrupting the computer program and storing for it a status or message code word into a specific memory location if it so desires. Five other types of interrupts that do not have an associated code word are provided. Each will cause program control to transfer to its unique memory location, from which response programs can be initiated.





UNIVAC CP-890/UYK MILITARY COMPUTER BLOCK DIAGRAM

REPERTOIRE OF INSTRUCTIONS

FUNCTION	INSTRUCTION CODE f (OCTAL)	INSTRUCTION	OVERLAPPED* EXECUTION TIME (MICROSECONDS)
LOGICAL	00	(Fault Interrupt)	1.8
	01	Right Shift Q	1.8
	02	Right Shift A	1.8
	03	Right Shift AQ	1.8
	04	Compare	1.8
	05	Left Shift Q	1.8
	06	Left Shift A	1.8
	07	Left Shift AQ	1.8
	40	Enter Logical Product	1.8
	41	Add Logical Product	1.8
	42	Subtract Logical Product	1.8
	43	Compare Masked	1.8
	44	Replace Logical Product	3.6
	45	Replace A+Logical Product	3.6
	46	Replace A—Logical Product	3.6
	47	Store Logical Product	1.8
	50	Selective Set	1.8
	51	Selective Complement	1.8
	52	Selective Clear	1.8
	53	Selective Substitute	1.8
LOAD	10	Enter Q	1.8
	11	Enter A	3.6
	12**	Enter Bj	3.6
INPUT/OUTPUT	13**	External Function on $\hat{Cj}$	1.8
	73**	Input Buffer on $\hat{Cj}$ (Without Monitor Mode)	3.6
	74**	Output Buffer on $\hat{Cj}$ (Without Monitor Mode)	3.6
	75**	Input Buffer on $\hat{Cj}$ (With Monitor Mode)	3.6
	76**	Output Buffer on $\hat{Cj}$ (With Monitor Mode)	3.6
	77 64	Enable Input CDM	1.8
	77 65	Enable Output CDM	1.8
	77 66	Disable Input CDM	1.8
	77 67	Disable Output CDM	1.8
	66	Terminate $\hat{Cj}$ Input Buffer Enable or Disable Interrupts	1.8
	67	Terminate $\hat{Cj}$ Output Buffer or All Buffers	1.8
	70**	Repeat	3.6

*For nonoverlapped, add 1.8 microseconds to the execution time.

**Execution time is constant—overlapped or not.

REPERTOIRE OF INSTRUCTIONS (CONT.)

FUNCTION	INSTRUCTION CODE f (OCTAL)	INSTRUCTION	OVERLAPPED* EXECUTION TIME (MICROSECONDS)
STORE	14	Store Q	1.8
	15	Store A	1.8
	16	Store Bj	3.6
	17**	Store $\hat{C}j$ or Test EFB	1.8
	32	Store A+Q	3.6
	33	Store A—Q	3.6
ARITHMETIC	20	Add A	1.8
	21	Subtract A	1.8
	22**	Multiply	7.2
	23**	Divide or Square Root	12.6 Divide 7.2 Square Root
	26	Add Q	1.8
	27	Subtract Q	1.8
	30	Enter Y+Q	1.8
	31	Enter Y—Q	1.8
REPLACE	24	Replace A+Y	3.6
	25	Replace A—Y	3.6
	34	Replace Y+Q	3.6
	35	Replace Y—Q	3.6
	36	Replace Y+1	3.6
	37	Replace Y—1	3.6
	54	Replace Selective Set	3.6
	55	Replace Selective Complement	3.6
	56	Replace Selective Clear	3.6
	57	Replace Selective Substitute	3.6
TRANSFER	60**	Jump (Arithmetic)	3.6
	61**	Jump (Manual)	3.6
	62**	Jump on $\hat{C}j$ Active Input Buffer	3.6
	63**	Jump on $\hat{C}j$ Active Output Buffer	3.6
	64**	Return Jump (Arithmetic)	5.4
	65**	Return Jump (Manual)	5.4
	71**	B Skip on Bj	3.6
	72**	B Jump on Bj	3.6

*For nonoverlapped, add 1.8 microseconds to the execution time.

**Execution time is constant—overlapped or not.

REPERTOIRE OF INSTRUCTIONS (CONT.)

FUNCTION	INSTRUCTION CODE f (OCTAL)	INSTRUCTION	OVERLAPPED* EXECUTION TIME (MICROSECONDS)
COMPUTER CONTROL FUNCTION	77 00	Enter Executive Mode	3.6
	77 01	Exit Executive Mode	3.6
	77 02	Load B and Jump	3.6
	77 03	Test Overflow Designator	3.6
	77 04	Enter Indirect Address Designator	1.8
	77 05	Execute Remote	1.8
	77 10	Enter Breakpoint Register	1.8
	77 12	Enter Display Register	1.8
	77 14	Store Breakpoint Register	1.8
	77 16	Store Display Register	1.8
	77 26	Set and Enable Monitor Clock	1.8
	77 32	Enter Status Register	1.8
	77 36	Store Status Register	1.8
	77 42	Sample Keyboard and Keyset	1.8
	77 43	Enter Memory Lockout Register	1.8
	77 44	Store Memory Lockout Register	1.8
	77 60	Enter Special Register	1.8
	77 61	Enter Input Extension Register	1.8
	77 62	Enter Output Extension Register	1.8
	77 63	Enter External Function Extension Register	1.8
	77 70	Store Special Register	1.8
	77 71	Store Input Extension Register	1.8
	77 72	Store Output Extension Register	1.8
	77 73	Store EF Extension Register	1.8
	77 74**	Disable Expanded Address Mode	1.8
	77 75**	Enable Expanded Address Mode	1.8
FLOATING POINT	77 07	Normalize AQ	3.6
	77 11	Double-Length Enter	3.6
	77 15	Double-Length Store	3.6
	77 20	Floating Point Add	7.2
	77 21	Floating Point Subtract	7.2
	77 22	Floating Point Multiply	10.8
	77 23	Floating Point Divide	16.2
	77 24	Double-Length Add	3.6
	77 25	Double-Length Subtract	3.6
	77 41	Floating Point Round Enable or Disable	1.8
Misc.	77 27	Test and Set Flag	3.6

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**Execution time is constant—overlapped or not.

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